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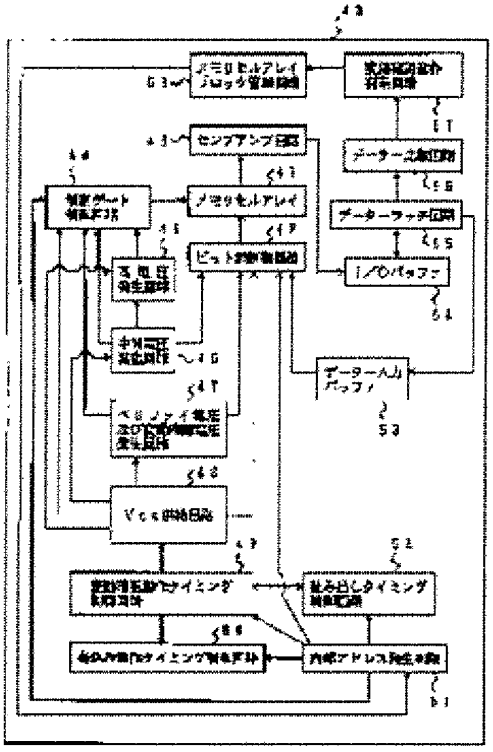
(54) SEMICONDUCTOR STORAGE DEVICE

(57)Abstract:
PURPOSE: To detect variation of a threshold value before data is destroyed and to correct it by changing a voltage applied to a word line, comparing read out data with each other, discriminating it as normal when both data are the same, discriminating it as that the threshold value is varied when they are different, and performing write-in again.
CONSTITUTION: A first voltage from a verification voltage/variation confirmation voltage generation circuit 47 is applied to a word line through a control gate control circuit 44, a memory cell array is selected and a memory cell is read out, and a first read-out result is latched in a data latch circuit 55, and in the same way, read-out data when high voltage is applied to a word line is compared with the resultant data by a data comparing circuit 56, further, data at the time of applying low voltage is compare with the first read-out data, and when a comparison result shows equality, the data is discriminated as normal by a variation confirmation operation judging circuit 57, when not, the data is discriminated as abnormal data for which a threshold value is varied without being destroyed, writing is performed again with voltage corresponding to an abnormal condition, and the data is corrected to a normal threshold value before data is destroyed.



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CLAIMS

[Claim(s)]
[Claim 1]When said threshold verification means detects changing a threshold of at least one or more cells among said two or more memory cells in a semiconductor memory device characterized by comprising the following, A semiconductor memory device possessing operation which performs re-writing to said cell in which a threshold is changed at least.
A memory cell array by which a memory cell has been arranged on a semiconductor layer at matrix form.
A threshold verification means to detect a threshold of two or more arbitrary memory cells in said memory cell array, or two or more memory cells in said memory cell array which are connected with the same word line at least.

[Claim 2]two or more arbitrary memory cells in a memory cell array characterized by comprising the following by which a memory cell has been arranged on a semiconductor layer at matrix form, and said memory cell array -- or, A semiconductor memory device provided with a threshold verification means to detect a threshold of two or more memory cells in said memory cell array connected with the same word line at least.
First operation that impresses the first voltage to a selection word line for a threshold state of said memory cell, and detects "1" data or "0" data by said verification means.
Second operation that impresses the second voltage higher than the first voltage to a selection word line for an upset condition of a threshold of two or more of said memory cells, and detects "1" data and "0" data by said verification means.
Third operation that impresses the third voltage lower than said first voltage to a selection word line, and detects "1" data and "0" data by said verification means.
Data in which data of at least one or more cells impressed said first voltage to a selection word line, and read it among said two or more memory cells, Fourth operation that performs re-writing to a cell which detects it as changing a threshold and is carrying out threshold change at least when data which impressed said second voltage to a selection word line, and read it is compared with data which impressed said third voltage to a selection word line, and read it and all are not in agreement.

[Claim 3]two or more arbitrary memory cells in a memory cell array characterized by comprising the following by which a memory cell has been arranged on a semiconductor layer at matrix form, and said memory cell array -- or, A semiconductor memory device provided with a threshold verification means to detect a threshold of two or more memory cells in said memory cell array connected with the same word line at least.
First operation that impresses the first voltage to a selection word line for a threshold state of said memory cell, and detects "1" data or "0" data by said verification means.
Second operation that impresses the second voltage that is different from the first voltage in an upset condition of a threshold of two or more of said memory cells to a selection word line, and

detects "1" data and "0" data by said verification means.
Data in which data of at least one or more cells impressed said first voltage to a selection word line, and read it among said two or more memory cells.
Third operation that performs re-writing to a cell which compares data which impressed said second voltage to a selection word line, and read it, detects it as changing a threshold and is carrying out threshold change at least when not in agreement.

[Claim 4]two or more arbitrary memory cells in a memory cell array characterized by comprising the following by which a memory cell has been arranged on a semiconductor layer at matrix form, and said memory cell array -- or, A semiconductor memory device provided with a threshold verification means to detect a threshold of two or more memory cells in said memory cell array connected with the same word line at least.
First operation that impresses the first voltage to a selection word line for a threshold state of said memory cell, and detects "1" data or "0" data by said verification means.
Second operation that impresses the second voltage higher than the first voltage to a selection word line for an upset condition of a threshold of two or more of said memory cells, and detects "1" data and "0" data by said verification means.
Third operation that impresses the third voltage lower than said first voltage to a selection word line, and detects "1" data and "0" data by said verification means.
The first data of a memory cell which gave and read the first voltage to said word line.
Fourth operation that detects having changed a threshold of a memory cell by comparing the second data of a memory cell which gave and read the second voltage higher than the first voltage to said word line.
Fifth operation that performs re-writing to a value higher than the second voltage to the above-mentioned cell at least when change is detected in said fourth operation.
By comparing the first data of a memory cell which gave and read the first voltage to said word line with the third data of a memory cell which gave and read the third voltage lower than the first voltage to said word line, The sixth operation that detects having changed a threshold of a memory cell, and seventh operation that performs re-writing to a value lower than the third voltage to the above-mentioned cell at least when change is detected in said sixth operation.

[Claim 5]Two or more data circuits which have a function to function as a sense amplifier and to memorize the inner first data of sensed information as data which controls a writing operation state of a memory cell, A writing means for performing writing operation according to the contents of said first data circuit respectively corresponding to two or more memory cells in said memory cell array simultaneously, A write verification means using said threshold detection means in order to check whether a state after writing operation of two or more of said memory cells is in a desired data storage state simultaneously, So that it may write in from the contents of the first data of a data circuit, and a state after writing operation of a memory cell and re-writing may be performed only to an insufficient memory cell, The contents mass update means of a data circuit which carries out the mass update of the contents of the data circuit, and said contents mass update means of a data circuit, Voltage of a bit line with which a state after writing operation of a memory cell is outputted is corrected according to the contents of the data circuit so that bit line voltage may be sensed / memorized as re-write data, A data circuit is operated as a sense amplifier, holding a data storage state of a data circuit and holding corrected bit line voltage until bit line voltage was corrected, Perform a mass update of the contents of the data circuit and writing operation based on the contents and the contents mass update of a data circuit of a data circuit, The semiconductor memory device according to claim 4 providing further the eighth operation that performs data writing electrically by carrying out repeating until a memory cell will be in a predetermined writing state.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to a nonvolatile semiconductor memory (EEPROM) rewritable electric especially with respect to a semiconductor memory device.
[0002]
[Description of the Prior Art]NAND type EEPROM which can be integrated highly is known as one of the EEPROMs. This carries out the series connection of two or more memory cells in the form which shares those sauce and a drain by adjoining things, and connects them to a bit line as one unit. A memory cell usually has the FETMOS structure where the charge storage layer and the control gate were laminated. Accumulation formation of the memory cell array is carried out into the p type well formed in the p type substrate or the n type substrate. The drain side of a NAND cell is connected to a bit line via a selector gate, and the sauce side is too connected to a common source line via a selector gate. The control gate of a memory cell is continuously allocated in a line writing direction, and serves as a word line.
[0003]The operation of this NAND cell type EEPROM is as follows. Data writing impresses high-tension Vpp1 (about =20V) to the control gate of the selected memory cell, The intermediate voltage Vppm (about =10V) is impressed to the control gate and selector gate of a non selection memory cell, and 0V or the intermediate voltage Vm (about =8V) is given to a bit line according to data. When 0V is given to a bit line, the voltage is transmitted to the drain of a select memory cell, and electron injection produces it in an electric charge accumulation layer. This shifts the threshold of the selected memory cell for Masakata. This state is set to "0." When Vm is given to a bit line, electron injection does not happen effectually, therefore a threshold does not change but stops at negative. This state is set to "1" by an erasing state. Data writing is simultaneously performed to the memory cell which shares a control gate.
[0004]Data erasure is simultaneously performed to all the memory cells in a NAND cell. That is, all the control gates are set to 0V, and a p type well is set to Vpp2 (about =20V). At this time, a selector gate, a bit line, and a source line are also set to 20V. Thereby, the electrons of a charge storage layer are emitted to a p type well by all the memory cells, and a threshold is shifted to a negative direction.
[0005]Data read sets the control gate of the selected memory cell to 0V, and is performed by detecting whether current flows by a select memory cell by making the control gate and selector gate of the other memory cell into the power supply voltage Vcc (for example, 5V).
[0006]From restrictions of reading operation, the threshold after "0" writing must be controlled between 0V and Vcc. For this reason, write verification is performed, only the memory cell of "0" writing shortage is detected, and re-write data is set up so that re-writing may be performed only to the memory cell of "0" writing shortage (the whole bit is verified). The memory cell of "0" writing shortage is detected by setting the selected control gate to 0.5V (verification voltage), and reading

it (verification read-out). That is, if the threshold of a memory cell has a margin to 0V and has not become more than 0.5V, current will flow by a select memory cell and it will be detected with "0" writing shortage. In the memory cell made into "1" writing state, since current naturally flows, the circuit called the verification circuit which compensates the current which flows through a memory cell is provided so that this memory cell may not be taken for "0" writing shortage. Write verification is performed at high speed by this verification circuit.

[0007]Repeating writing operation and write verification, writing time is optimized to each memory cell by carrying out data writing, and the threshold after "0" writing is controlled between Vcc(s) from 0V.

[0008]By controlling a threshold between 0V and Vcc, NOR type EEPROM considers it as "1" data, and is taken as "0" data by controlling a threshold more than Vcc.

[0009]thus -- setting EEPROM at the time of data writing -- "0" and "1" -- it is alike, respectively, and it receives and a threshold is set up appropriately. However, it changes as time is formed as for the threshold of a memory cell. For example, since the electric charge of a charge storage layer decreases according to the leakage current of the surrounding insulator layer of a charge storage layer by being neglected after data is written in, it will change from the threshold set up appropriately to a neutral threshold. For example, in the case of NAND type EEPROM, if a neutral threshold shall be about 0.5 v, "1" data turns into "0" data, in the case of NOR type EEPROM, "0" data will turn into "1" data and data will be destroyed. Since it reads and Vcc voltage is sometimes impressed to a non selection cell, an electron is poured into a charge storage layer, "1" data turns into "0" data, and NAND type EEPROM has the problem that data is destroyed.

[0010]On the other hand, as mentioned above, even if it performs verification writing the whole bit, a threshold may be unable to be set as the predetermined range. For example, in NAND type EEPROM, "0" data is written in a selection cell and the threshold presupposes then that it became more than Vcc (for example, 7V). Next, in a non selection cell, though another cell of a NAND cell containing said selection cell is chosen and it tries to read data, since the cell more than Vcc exists, a threshold, Since cell current does not flow, in order to always read with "0" data regardless of the data of a selection cell, there is a problem of becoming poor.

[0011]Thus, in a nonvolatile semiconductor memory, there were a problem that data will be destroyed, and a problem of carrying out erroneous read if a threshold cannot be set as the predetermined range, by neglecting the written-in data.

[0012]

[Problem(s) to be Solved by the Invention]In the conventional nonvolatile semiconductor memory, there were a problem that data will be destroyed, and a problem of carrying out erroneous read if a threshold cannot be set as the predetermined range, by neglecting the written-in data as mentioned above.

[0013]The place which this invention was made in consideration of the above-mentioned situation, and is made into the purpose, This data by carrying out re-writing to the same block or another block by detecting change of the threshold of a memory cell and reading this data, The operation which makes it possible to set a threshold as the predetermined range and to avoid destruction of data, When it cannot be set as a predetermined threshold within the limits, this data by carrying out re-writing to the same block or another block by reading this data, It is in providing the semiconductor memory device possessing the operation which makes it possible to set a threshold as the predetermined range and to avoid erroneous read.

[0014]

[Means for Solving the Problem]In order to solve an aforementioned problem, a semiconductor memory device of this invention, two or more arbitrary memory cells in a memory cell array by which a memory cell has been arranged on a semiconductor layer at matrix form, and said memory cell array -- or, In a semiconductor memory device provided with a threshold verification means to detect a threshold of two or more memory cells in said memory cell array connected with the same

word line at least. When changing a threshold of at least one or more cells among said two or more memory cells is detected by said threshold verification means, it is characterized by providing operation which performs re-writing to said cell in which a threshold is changed at least.
[0015]A threshold state of two or more memory cells which stand in a row in the same word line in a memory cell array by impressing the first voltage to a selection word line specifically, The first operation that detects "1" data or "0" data, and the second operation that detects an upset condition of a threshold of two or more of said memory cells by impressing the second voltage higher than the first voltage to a selection word line, The third operation detected by impressing the third voltage lower than the first voltage to a selection word line, By comparing the first data of a memory cell which gave and read the first voltage to said word line with the second data of a memory cell which gave and read the second voltage higher than the first voltage to said word line, In a case where it is detected as the fourth operation that detects having changed in the direction with a small threshold of a memory cell, The fifth operation that fluctuates a threshold of the above-mentioned cell to a value higher than the second voltage, By comparing the first data of a memory cell which gave and read the first voltage to said word line with the third data of a memory cell which gave and read the third voltage lower than the first voltage to said word line, The sixth operation that detects having changed in the direction with a large threshold of a memory cell, When it detects, it is characterized by providing the seventh operation that fluctuates a threshold of the above-mentioned cell to a value lower than the third voltage.
[0016]While a threshold cannot be controlled in a predetermined range as erroneous read prevention, When a threshold is greatly set up across a prescribed range, With operation which impresses larger voltage than predetermined read voltage to a word line, and reads data, when a threshold is set up smaller than a prescribed range, Operation which impresses voltage smaller than predetermined read voltage to a word line, and reads data, and operation which carries out re-writing for this data to another block or the same block are provided.
[0017]
[Function]By impressing the second voltage higher than the first voltage to a word line, reading a cell data in this invention, and comparing the cell data which impressed the first voltage to the word line and read it, When it judges that it is set as the range normal when these data is the same and these data differs on the other hand, data corruption has not been carried out, but it can be detected as carrying out threshold change enough. By impressing the third voltage lower than the first voltage to a word line, reading a cell data, and comparing the cell data which impressed the first voltage to the word line and read it, When it judges that it is set as the range normal when these data is the same and these data differs on the other hand, data corruption has not been carried out, but it can be detected as carrying out threshold change enough. When detected as changing the threshold of a cell enough, re-writing is performed for data so that it may return to the original threshold of each cell. Thus, according to this invention, by threshold change, before data breaks, the threshold change is detected and it is corrected to the controlled original threshold.
[0018]The next operation is performed while the threshold cannot be controlled in the predetermined range as erroneous read prevention. That is, when a threshold is greatly set up across a prescribed range, operation which impresses larger voltage than predetermined read voltage to a word line, and reads data is performed. When a threshold is set up smaller than a prescribed range, operation which impresses voltage smaller than predetermined read voltage to a word line, and reads data is performed. In NAND type EEPROM for example, by using this appearance, Though "0" data is written in a selection cell and the threshold has become more than Vcc (for example, 7V), Next, since sufficiently big voltage is impressed to the word line of this non selection cell even if the cell more than Vcc exists in a non selection cell in a threshold when another cell of a NAND cell containing said selection cell is chosen and data is read, it becomes possible to read the data of a selection cell correctly. this read data -- another block -- or the threshold of a memory cell can be set as the predetermined range by performing operation which

carries out re-writing to the same block.

[0019]

[Example]Hereafter, an example is described, referring to drawings. Drawing 1 shows the superficial layout of the memory cell array of NAND cell type EEPROM concerning the first example of this invention, and drawing 2 and drawing 3 (a) and (b) show A-A' of drawing 1, and B-B' and the sectional view which met the C-C' line, respectively. The memory cell array of this example is formed on p type well 2b further formed in the n type well 2a formed on the p type semiconductor substrate 1 as shown in drawing 2. A memory cell may be directly formed on a p type semiconductor substrate.

[0020]In drawing 2, on p type well 2b, the charge storage layer 4 is formed via the 1st gate dielectric film 3, and the control gate 6 is further formed via the 2nd gate dielectric film 5. The n type diffused layers 7 are formed, it becomes the sauce and the drain area which the adjoining cell shares, and the memory cells M1-M4 connected in series are formed in the surface of said p type well 2b inserted into these lamination gate electrodes. The selection transistor S1 and S2 which have the selector gate 11 of a lamination type via gate-dielectric-film 3' on a p type well are formed in the right and left of these memory cells. On the control gate 6 and the selector gate 11, the bit line (BL) 10 is formed via the interlayer insulation film 9, the bit contacts 13 are led, and it is n+. It is connected to diffusion-zone 7'.

[0021]Although drawing 1 is the top view in which two rows of memory cell arrays like the above were shown, it is continuously connected to a transverse direction and the control gate 6 of the memory cell arranged in parallel serves as the control gate lines (word line) CG1-CG4. It is continuously connected to a transverse direction and the selector gate 11 is also set to selection gate line SG1 (drain side) and SG2 (sauce side). Between the selection transistor S1 connected to the bit line BL, and the selection transistor S2 connected to the common source line Vs, the series connection of the four memory cells M1-M4 is carried out, and they constitute one NAND cell. The selection transistor S1 and S2 have the selector gate SG. Like the above-mentioned, each memory cell has the floating gate 4 and the control gate 6 by which laminating formation was carried out, and memorizes information in the quantity of the electric charge stored in the floating gate 4. The quantity of this stored electric charge can be read as a threshold of a memory cell.

[0022]In this invention, detection of this threshold change is performed by the voltage impressing method shown in drawing 4 (a), (b), and (c). Here, the memory cell M2 which has control gate CG2 is chosen. Read to selection word line CG2 and the voltage 0.5V is impressed so that drawing 4 (a) may see, To non selection word line CG1, CG3, CG4 and the selection transistor S1, selector-gate SG1 of S2, and SG2, Vcc, For example, 5V is impressed, the common source line Vs, the p type substrate 1, and p type well 2b are grounded to 0V, and the bit line BL is precharged to Vcc and made into floating.

[0023]The threshold of the selection cell M2 reads, at this time, if it is more than voltage 0.5V, cell current does not flow, but the voltage of the bit line BL, The threshold of the selection cell M2 reads, on the other hand, it is maintained, if it is less than voltage 0.5V, cell current flows, and the voltage of the bit line BL is set to 0V from a precharge level, has the voltage difference of this bit line, and detects it with a sense amplifier. At this time, use the time of bit line voltage being set to 0V as "1" data, and let one side be "0" data. Then, the read data of the detected cell is transmitted to latch circuitry from a sense amplifier, and latch circuitry is separated from a sense amplifier.

[0024]Next, while transmitting the latched data to I/O, the threshold fluctuation level shown below is checked. The first change check voltage 0.0V is impressed to selection word line CG2 so that drawing 4 (b) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs, the p type substrate 1, and p type well 2b are grounded to 0V, and the bit line BL is precharged to Vcc and made into floating.

[0025]At this time, if the threshold of the selection cell M2 is first more than change check voltage 0.0V, cell current does not flow, but the voltage of the bit line BL, It is maintained, on the other

hand, if the threshold of the selection cell M2 is less than the first change check voltage 0.0V, cell current flows, and the voltage of the bit line BL is set to 0V from a precharge level. It has the voltage difference of this bit line, and the first change confirmation data is detected with a sense amplifier.

[0026]Next, the second change check voltage 1.0V is impressed to selection word line CG2 so that drawing 4 (c) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs, the p type substrate 1, and p type well 2b are grounded to 0V, and the bit line BL is precharged to Vcc and made into floating.

[0027]At this time, if the threshold of the selection cell M2 is second more than change check voltage 1.0V, cell current does not flow, The voltage of the bit line BL is maintained, on the other hand, if the threshold of the selection cell M2 is less than the second change check voltage 1.0V, cell current flows, and the voltage of the bit line BL is set to 0V from a precharge level. It has the voltage difference of this bit line, and the second change confirmation data is detected with a sense amplifier. At this time, as shown in Table 1, a classification and a detection result can be judged.

[0028]

[Table 1]

しきい値状態	読み出しデータ 図4(a)	第1の変化確認データ 図4(b)	第2の変化確認データ 図4(c)	検知の結果
1.0V<Vth	"0"	"0"	"0"	正常
0.5V<Vth≦1.0V	"0"	"0"	"1"	電子が放出された異常
0.0V<Vth≦0.5V	"1"	"0"	"1"	電子が注入された異常
0.0V>Vth	"1"	"1"	"1"	正常

First, read data is "0" when the threshold of a cell is more than 1.0V.
And the first change confirmation data is "0", and the second change confirmation data is set to "0."
Read data is "0" when the thresholds of a cell are more than 0.5V and less than 1.0V.
And the first change confirmation data is "0", and the second change confirmation data is set to "1."
Read data is "1" when the thresholds of a cell are more than 0.0V and more than 0.5V.
And the first change confirmation data is "0", and the second change confirmation data is set to "1."
Read data is "1" when the threshold of a cell is less than 0.0V.
And the first change confirmation data is "1", and the second change confirmation data is set to "1."

[0029]Below, the corrective action method for each of above-mentioned classifications is explained. First, when the read-out data, first, and second change confirmation data is "0", originally "0" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made. When the read-out data, first, and second change confirmation data is "1", originally "1" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made.

[0030]On the other hand, read-out data and the first change confirmation data are "0", when the second change confirmation data is "1", originally "0" data is written in, but the threshold is changed from the positive threshold to the negative threshold.
It is not judged that the variation is large enough and data-hold is carried out normally, but re-writing is performed to a memory cell so that a threshold may be again shifted to a positive direction.

At this time, it is preferred to use the threshold more than said second change check voltage.
[0031]Read-out data and the second change confirmation data are "1", when the first change confirmation data is "0", originally "1" data is written in, but the threshold is changed from the negative threshold to the positive threshold.
It is not judged that the variation is large enough and data-hold is carried out normally, but re-writing is performed to a memory cell so that a threshold may be again shifted to a negative direction.
At this time, it is preferred to use the threshold below said first change check voltage. The sequence stated above is collectively shown in drawing 5.
[0032]Next, the re-writing operation performed according to the above-mentioned judgment is explained. Although only the cell which became poor may be re-written in, it does not matter even if it re-writes in the whole cell block containing the cell which became poor. When re-writing in for every cell block, the data in a cell block may be read once, and it may re-write in in the same cell block according to this data, and may re-write in in another cell block. The above-mentioned cell block may define it as two or more cells connected with the same word line, and may define it as two or more NAND cell blocks connected with the same word line. When abnormalities are detected by data fluctuation check operation following on the usual data reading operation, In order to go into re-writing operation, by setting a flag etc. shows that a chip state is in relief operation out of the chip by a chip being a waiting state like the usual method.
[0033]Whenever the data fluctuation check operation described above performs read operation of the selected cell data, may perform it to the cell block containing the selection cell and its selection cell, and, It is managed by the timer currently installed in a chip and out of the chip, and when predetermined time comes, it may be made to carry out to all the cells. Or when it is managed by the counter which counts the number of times of data read currently installed in a chip and out of the chip and only the predetermined number of times reads, it may be made to carry out to the cell or the cell block containing the cell. Although drawing 6 shows the block diagram of the card 20 containing CPU21 and the memory chip 22, The above-mentioned timer 23 or the counter 24 operates by an external power, when the external power 26 is supplied to the card, and when the external power is not supplied, it may be made to operate by the cell 25 installed on the card.
[0034]The card system based on the first example described above is shown in drawing 7. That is, the external device is connected to the controller (CPU) 32 of the card system 30 via the interface 31. The memory system 40 is connected with this CPU32 and the internal battery 33 to the timer 34. The method of operating within this memory system 40 about the case where it has the NAND type EEPROM cellular structure as memory structure. It explains to another block which leads the whole cell block connected with the same word line containing not only the cell that became poor but the cell which became poor to another word line taking the case of the case where re-writing is performed. Although a memory system here may comprise a single memory chip, it may serve as external out of a chip of a part of functions.
[0035]Drawing 8 is a block diagram showing the internal configuration of the memory system 40. First, the cell block which performs a data fluctuation check is chosen, by the internal address generation circuit 51, the memory chip which should check data is chosen and the control gate and bit line of the inside are chosen further. And after precharging all the bit lines connected to the cell block to Vcc voltage by the read timing control circuit 52, Read voltage, for example, 0.5V, is impressed to the selection-control gate in a selection NAND cell, and Vcc voltage, for example, 3.3V, is impressed to it at the non selection control gate in a selection NAND cell, and the selector gate in a selection NAND cell. And data is read for the voltage of each bit line by the sense amplifier circuit 43, the result is put into I/O buffer 54, and data is latched to the data latch circuit 55 as read data.
[0036]Next, after precharging all the bit lines connected to the cell block to Vcc voltage by a change check operation timing control circuit, The first change check voltage, for example, 0.0V, is

impressed to the selection-control gate in a selection NAND cell, and Vcc voltage, for example, 3.3V, is impressed to it at the non selection control gate in a selection NAND cell, and the selector gate in a selection NAND cell. And data is read for the voltage of each bit line by the sense amplifier circuit 43, the result is put into I/O buffer 54, and data is latched to the data latch circuit 55 as first change confirmation data.
Then, after precharging all the bit lines connected to the cell block to Vcc voltage, The second change check voltage, for example, 1.0V, is impressed to the selection-control gate in a selection NAND cell, and Vcc voltage, for example, 3.3V, is impressed to it at the non selection control gate in a selection NAND cell, and the selector gate in a selection NAND cell.
And data is read for the voltage of each bit line by the sense amplifier circuit 43, the result is put into I/O buffer 54, and data is latched to the data latch circuit 55 as second change confirmation data.
[0037]Next, the data comparator circuit 56 compares the value of the read data latched in the data latch circuit 55, the first change confirmation data, and the second change confirmation data. The change check operation judging circuit 57 processes the comparison result, as shown below. When all the read-out data, first, and second change confirmation data is "0", Originally "0" data is written in, and when all the read-out data, first, and second change confirmation data is "1", originally "1" data is written in, and it judges that data-hold is both carried out normally, and change check operation is ended. Read-out data and the first change confirmation data are "0", when the second change confirmation data is "1", originally "0" data is written in, but it is judged that a threshold is changed sharply. Read-out data and the second change confirmation data are "1", when the first change confirmation data is "0", originally "1" data is written in, but it is judged that a threshold is changed sharply.
[0038]As mentioned above, when the cell in which the threshold is changed is detected by the change check operation judging circuit 57, the flag which shows that a chip state is in a relief state is set, and the re-writing of data is performed in the procedure shown below. It assigns to the cell in the cell block which was protected by having made said selection cell block into the defective block, chose the following cell block, and chose the cell address in a former selection cell block by the memory cell array block control circuit this time. And 0V is impressed to all the control gates in a new selection cell block by the writing operation timing control circuit 50, By the high voltage generation circuit 45, the high tension for elimination, for example, about 20V, is impressed to all the selector gates, the p type well, the n-type semiconductor board (SUB), and all the selector gates in a non selection cell block, and all the cells in a selection cell block are eliminated to them.
[0039]Next, in order to check an erasing state, erase verifying operation requires. Said erasing operation and erase verifying operation are repeated, and are performed until it impresses erasure verifying voltage to all the control gates in a selection cell block, it reads data according to the usual read-out procedure and all the data turns into "1" data. At this time, it is most desirable to use the first change check voltage especially, using the voltage below the first change check voltage as erasure verifying voltage. Next, to the selection-control gate in a new selection cell block by the writing operation timing control circuit 50 by the high voltage generation circuit 45. Impress the high tension for writing, for example, about 20V, and to the non selection control gate in a new selection cell block by the intermediate voltage generating circuit 46. Impress intermediate voltage, for example, about 10V, and to each bit line. If it is "1" data, intermediate voltage, for example, about 7V, is impressed by said intermediate voltage generating circuit 46, according to the data read data latched in said data latch circuit, if it is "0" data, 0V is impressed, and data is written in.
[0040]Next, in order to check a writing state, write verification operation requires. Impress write verification voltage to the selection-control gate in a selection cell block, and in a non selection control gate. Said writing operation and write verification operation are repeated, and are performed until it impresses Vcc, it reads data according to the usual read-out procedure and all the data is in agreement with read data. At this time, it is most desirable to use the second change check voltage

especially, using the voltage more than the second change check voltage as write verification voltage. By the above, re-writing operation brings down the flag which shows that it ends and is in a relief state, and ends all the change check operations.

[0041]Although the above example is performed by [with read data] carrying out ternary comparison using the first and second change check voltage, When the changing direction of the threshold of a cell is decided, it is good in a line by carrying out binary comparison by using only either the first change check operation or the second change check operation. Below, it states concretely.

[0042]Next, the second example in connection with this invention is described. It performs the detection by a ****** case that this example changes the threshold of a cell in the direction of smallness by the voltage impressing method shown in drawing 9 (a) and (b). Here, the memory cell M2 which has control gate CG2 is chosen. Read to selection word line CG2 and the voltage 0.5V is impressed so that drawing 9 (a) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs and a p type substrate, or a p type well is grounded to 0V, and the bit line BL is precharged to Vcc and made into floating. At this time, the threshold of the ****** cell M2 reads, and, in the case of beyond voltage 0.5V, it does not flow through cell current, but the voltage of the bit line BL is maintained. On the other hand, the threshold of the selection cell M2 reads, in the case of not more than voltage 0.5V, cell current flows, the voltage of the bit line BL is set to 0V from a precharge level, and a sense amplifier detects the voltage difference of this bit line. At this time, use the time of bit line voltage being set to 0V as "1" data, and let another side be "0" data. Then, the read data of the detected cell is transmitted to latch circuitry from a sense amplifier, and latch circuitry is separated from a sense amplifier.

[0043]Next, while transmitting the latched data to I/O, the threshold fluctuation level shown below is checked. The first change check voltage 0.0V is impressed to selection word line CG2 so that drawing 9 (b) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs, the p type substrate 1, and p type well 2b are grounded to 0V, and the bit line BL is precharged to Vcc and made into floating. At this time, if the threshold of the selection cell M2 is first more than change check voltage 0.0V, cell current does not flow, but the voltage of the bit line BL, It is maintained, on the other hand, if the threshold of the selection cell M2 is less than the first change check voltage 0.0V, cell current flows, and the voltage of the bit line BL is set to 0V from a precharge level. It has the voltage difference of this bit line, and the first change confirmation data is detected with a sense amplifier. At this time, a classification and a detection result as shown in Table 2 can be judged.

[0044]

[Table 2]

しきい値状態	読み出しデータ 図9(a)	第1の変更確認データ 図9(b)	検知の結果
0.5V<Vth	"0"	"0"	正常
0.0V<Vth≦0.5V	"1"	"0"	電子が注入された異常
0.0V>Vth	"1"	"1"	正常

First, read data is "0" when the threshold of a cell is more than 0.5V.
And the first change confirmation data is "0."
Read data is "1" when the thresholds of a cell are more than 0.0V and more than 0.5V.
And the first change confirmation data is "0."
Read data is "1" when the threshold of a cell is less than 0.0V.
And the first change confirmation data is "1."

[0045]Below, the corrective action method for the above-mentioned classification is explained. First, when read-out data and the first change confirmation data are "0", originally "0" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made. When read-out data and the first change confirmation data are "1", originally "1" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made.
[0046]Read-out data is "1", the first change confirmation data is "0", and, in **, originally "1" data is written in, but the threshold is changed from the negative threshold to the positive threshold. It is not judged that the variation is large enough and data-hold is carried out normally, but the re-writing of data is performed like a last example.
Although the erasure verifying voltage used at the time of said erase verifying operation performed at this time may be below the first change check voltage, it is desirable to use the same voltage as the first change check voltage especially. As for the write verification voltage used at the time of said write verification operation, it is desirable to use the same voltage as read voltage. The sequence of the operation described above is collectively shown in drawing 10.
[0047]Next, the third example in connection with this invention is described. It performs the detection by a ****** case that this example changes the threshold of a cell in the adult direction by the voltage impressing method shown in drawing 9 (c) and (d). Here, the memory cell M2 which has control gate CG2 is chosen. Read to selection word line CG2 and the voltage 0.5V is impressed so that drawing 9 (c) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs, the p type substrate 1, and p type well 2b are grounded to 0V, and the bit line BL is precharged to Vcc and made into floating. At this time, the threshold of the selection cell M2 reads, and, in the case of beyond voltage 0.5V, it does not flow through cell current, but the voltage of the bit line BL is maintained. On the other hand, the threshold of the selection cell M2 reads, in the case of not more than voltage 0.5V, cell current flows, the voltage of the bit line BL is set to 0V from a precharge level, and a sense amplifier detects the voltage difference of this bit line. At this time, use the time of bit line voltage being set to 0V as "1" data, and let one side be "0" data. Then, the read data of the detected cell is transmitted to latch circuitry from a sense amplifier, and latch circuitry is separated from a sense amplifier.
[0048]Next, the second change check voltage 1.0V is impressed to selection word line CG2 so that drawing 9 (d) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs and a p type substrate, or a p type well is grounded to 0V, and the bit line BL is precharged to Vcc and made into floating. At this time, when the threshold of the selection cell M2 is second more than change check voltage 1.0V, cell current does not flow, but the voltage of the bit line BL is maintained. On the other hand, when the threshold of the selection cell M2 is less than the second change check voltage 1.0V, cell current flows, and the voltage of the bit line BL is set to 0V from a precharge level. It has the voltage difference of this bit line, and a sense amplifier detects the second change confirmation data. At this time, a classification and a detection result as shown in Table 3 can be judged.
[0049]
[Table 3]

しきい値状態	読み出しデータ 図9(c)	第2の変更確認データ 図9(d)	検知の結果
1.0V<Vth	"0"	"0"	正常
0.5V<Vth≦1.0V	"0"	"1"	電子が放出されない
Vth≦0.5V	"1"	"1"	正常

First, read data is "0" when the threshold of a cell is more than 1.0V.
And the second change confirmation data is set to "0."
Read data is "0" when the thresholds of a cell are more than 0.5V and less than 1.0V.
And the second change confirmation data is set to "1."
Read data is "1" when the threshold of a cell is less than 0.5V.
And the second change confirmation data is set to "1."

[0050]Below, the corrective action method for the above-mentioned classification is shown. First, when read-out data and the second change confirmation data are "0", originally "0" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made. When read-out data and the second change confirmation data are "1", originally "1" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made.
[0051]On the other hand, read-out data is "0", the second change confirmation data is "1", and, in **, originally "0" data is written in, but the threshold is changed from the positive threshold to the negative threshold.
It is not judged that the variation is large enough and data-hold is carried out normally, but the re-writing of data is performed like a last example.
As for the erasure verifying voltage used at the time of said erase verifying operation performed at this time, it is desirable to use the same voltage as read voltage. Although more than the second change check voltage may be sufficient as the write verification voltage used at the time of said write verification operation, it is desirable to use the same voltage as the second change check voltage especially. The sequence of the operation described above is collectively shown in drawing 11.
[0052]Only the size relation is important, and may make which voltage reference voltage, such as 0V and Vcc, and the read voltage described above, the first change detection voltage, and the second change detection voltage may apply NOR type EEPROM and a memory cell to AND type EEPROM connected in parallel.
[0053]Next, the circuit for realizing this invention concretely is explained. Drawing 12 is a precharge circuit, a write-in change confirmation circuit, an elimination change confirmation circuit, and an example of a circuit that includes a verification circuit, a sense amplifier and data latch circuit, and a package detecting circuit the whole bit. It writes in by p channel MOS transistorTr2 and Tr3, a change confirmation circuit is constituted, and the elimination change confirmation circuit comprises n channel MOS transistorTr4 and Tr5.
[0054]Drawing 13 is a circuit diagram for explaining detection of the abnormal data explained in drawing 4 and Table 1, and is taken as n=i, j, k, and l in a figure. i corresponds, when the read-out data [of the memory cell M2i], first, and second change confirmation data is "0" (i.e., when not making data correction to M2i by the case where "0" data is originally written in and data-hold of it is carried out normally).
[0055]The read-out data of the memory cell M2j and the first change confirmation data are "0", when the second change confirmation data is "1", originally the data of "0" is written in, but j. It corresponds, when performing re-writing to the memory cell M2j by the case where the threshold is changed from the positive threshold to the negative threshold so that a threshold may be again shifted to a positive direction.
[0056]The read-out data of the memory cell M2k and the second change confirmation data are "1", when the first change confirmation data is "0", originally the data of "1" is written in, but k. It corresponds, when performing re-writing to the memory cell M2k by the case where the threshold is changed from the negative threshold to the positive threshold so that a threshold may be again shifted to a negative direction.
[0057]It corresponds, when the read-out memory cell [M2l.] data, first, and second change confirmation data of l is "1" (i.e., when not making data correction to M2l. by the case where the

data of "1" is originally written in and data-hold of it is carried out normally).
[0058]Although the data of "1" is originally written in the memory cell M2k, drawing 14 and 15 divide a detection pickpocket operation timing figure two, and show the case where the threshold is changed from the negative threshold to the positive threshold. If the signal PRSTD for bit line reset changes from Vcc to Vss at first and bit line precharge signal PREB changes from Vcc to Vss, the bit line BLi, BLj, BLk, and BLl will be charged to bit line precharge level VR. At this time, the bit line transfer gate signal BLCD changes from Vss to Vcc, and the verification nodes VRYi, VRYj, and VRYk and VRYl are also charged to VR. Next, if control gating signal CG2 reads and control gating signal CG1 of others, CG3, CG4, selector-gate signal SG1, and SG2 are set to Vcc on the voltage VREAD (for example, 0.5V), the memory cell M2i, M2j, M2k, and M2l. will be read.
[0059]As for the memory cell M2i and M2j, originally "0" is written, since "1" is originally written, only the bit line BLkBLl is discharged and M2k and M2l. change from VR to Vss. When the control signal SEN of a sense amplifier and RLCH are set to Vcc from Vss after that and SENB and RLCHB are set to Vss from Vcc, Vcc is made the verification nodes VRYi and VRYj and Vss is latched to VRYk and VRYl (memory).
[0060]In order to read by the first check voltage VREF1 again after that, the bit line transfer gate signal BLCD is set to Vss from Vcc, and a bit line is separated from a verification node, and is charged to VR after bit line reset.
[0061]Next, if the first check voltage VREF1 (for example, 0V), control gating signal CG1 of others, CG3, CG4, selector-gate signal SG1, and SG2 turn into control gating signal CG2 to Vcc, the memory cell M2i, M2j, M2k, and M2l. will be read. Since the memory cell M2k is changed from the threshold negative in a threshold to the positive threshold at this time, the bit line BLk is not discharged. Other bit lines are the same as the case where read to the control gating signal CG2 [last], and the voltage VREAD is impressed and read.
[0062]Next, comparison with the last read-out data starts. The last read-out data is latched to the verification nodes VRYi, VRYj, and VRYk and VRYl. If the elimination acknowledge signal REFE of an elimination confirmation circuit is set to Vcc from Vss, the bit line BLiBLj is set to Vss from VR, and since the bit line BLl is Vss, only the bit line BLk will maintain precharge level VR. If the bit line transfer gate BLCD is set to Vcc from Vss after that and a bit line and a verification node connect too hastily, the bit line BLiBLj will become Vss+beta, BLk will become VR-alpha, and BLl will be set to Vss. When alpha and beta set capacity of a bit line and a verification node to CB and CVRY here, respectively, it is VR-alpha =-VRxCB/(CB+CVRY).
Vss+beta = (VccxCVRY)/(CB+CVRY)
It comes out, it is, and since CB is far large as compared with CVRY, VR-alpha becomes almost equal to VR, and Vss+beta is set to about 0 v.
[0063]Next, if the sense amplifier control signal SEN and RLCH are set to Vcc from Vss and SENB and RLCHB are set to Vss from Vcc, only the verification node VRYk will be set to Vcc and other VRYi(s), VRYj, and VRYl will be set to Vss. If package detection reset-signal VSTIN is set to Vss from Vcc after that and the elimination detection signal AECON is set to Vcc from Vss, SENSE will be set to Vss from Vcc and will tell the abnormalities in read-out. If the abnormalities in read-out are told, the re-writing of a memory cell will start.
[0064]Although the data of "0" is originally written in the memory cell M2j, drawing 16 and 17 divide a detection pickpocket operation timing figure two, and show the case where the threshold is changed from the positive threshold to the negative threshold. If the signal PRSTD for bit line reset changes from Vcc to Vss at first and bit line precharge signal PREB changes from Vcc to Vss, the bit line BLi, BLj, BLk, and BLl will be charged to bit line precharge level VR. At this time, the bit line transfer gate signal BLCD changes from Vss to Vcc, and the verification nodes VRYi, VRYj, and VRYk and VRYl are also charged to VR. Next, if control gating signal CG2 reads and control gating signal CG1 of others, CG3, CG4, selector-gate signal SG1, and SG2 are set to Vcc on the voltage VREAD (for example, 0.5V), the memory cell M2i, M2j, M2k, and M2l. will be read.

[0065]As for the memory cell M2i and M2j, originally "0" is written, since "1" is originally written, only the bit line BLkBLl is discharged and M2k and M2l. change from VR to Vss. When the control signal SEN of a sense amplifier and RLCH are set to Vcc from Vss after that and SENB and RLCHB are set to Vss from Vcc, Vcc is made the verification nodes VRYi and VRYj and Vss is latched to VRYk and VRYl (memory).
[0066]In order to read by the second check voltage VREF2 again after that, the bit line transfer gate signal BLCD is set to Vss from Vcc, and a bit line is separated from a verification node, and is charged to VR after bit line reset.
[0067]Next, if the second check voltage VREF2 (for example, 1V), control gating signal CG1 of others, CG3, CG4, selector-gate signal SG1, and SG2 turn into control gating signal CG2 to Vcc, the memory cell M2i, M2j, M2k, and M2l. will be read. Since the memory cell M2j is changed from the threshold positive in a threshold to the negative threshold at this time, the bit line BLj is discharged. Other bit lines are the same as the case where read to the control gating signal CG2 [last], and the voltage VREAD is impressed and read.
[0068]Next, comparison with the last read-out data starts. The last read-out data is latched to the verification nodes VRYi, VRYj, and VRYk and VRYl. If the write-in acknowledge signal REFP of a write-in confirmation circuit is set to Vss from Vcc, the bit line BLkBLl is set to Vss from Vss, and since the bit line BLj is Vss, only the bit line BLi will maintain precharge level VR. If the bit line transfer gate BLCD is set to Vcc from Vss after that and a bit line and a verification node connect too hastily, the bit line BLkBLl will become Vcc-alpha, BLj will become Vss+beta, and BLi will be set to Vss. When alpha and beta set capacity of a bit line and a verification node to CB and CVRY here, respectively, it is Vcc-alpha =-(VccxCB)/(CB+CVRY).
Vss+beta = (VccxCVRY)/(CB+CVRY)
It comes out, it is, and since CB is far large as compared with CVRY, Vcc-alpha becomes almost equal to Vcc, and Vss+beta is set to about 0 v.
[0069]Next, if the sense amplifier control signal SEN and RLCH are set to Vcc from Vss and SENB and RLCHB are set to Vss from Vcc, only the verification node VRYj will be set to Vss and other VRYi(s), VRYk, and VRYl will be set to Vcc. If package detection reset-signal VSTIN is set to Vss from Vcc after that and the write-in detection signal APCON is set to Vcc from Vss, SENSE will be set to Vss from Vcc and will tell the abnormalities in read-out. If the abnormalities in read-out are told, the re-writing of a memory cell will start.
[0070]Drawing 18 and 19 divide the circuit block of a core part two, and show it, the blocks h and i are blocks of the spare for rewrites, and the other blocks d, e, and f and g are usually blocks. Now, the case where the abnormalities in read-out occur with the block d is considered. In this case, the stored data of the block d is copied to the SUPEA block h for re-writing, and the rewrite of the contents of the block h is carried out for the block d to the block d after block deletion. That is, after carrying out block deletion of the spare block h first, it reads from control gate line CGd4 of the block d by read voltage VREAD. At this time, there are no abnormalities in read data, and even if there is change of a threshold, it is read correctly. These contents are latched to the sense-amplifier and data latch circuit DLj, DLk, and DLl. Control gate line CGh4 is chosen and the data latched to this sense-amplifier and data latch circuit DLj, DLk, and DLl is written in. This is repeated successively and the stored data about control gate line CGd4, CGd3, CGd2, and CGd1 is written in control gate line CGh4, CGh3, CGh2, and CGh1. Then, the contents of the stored data of the SUPEA block h are conversely re-written for the block d in the block d after block deletion.
[0071]When not block deletion but elimination of each page unit can be performed, Even if it does not use the SUPEA blocks h and i, it reads one contents about each control gate line of the block d at a time to the sense amplifier and data latch circuit DLj, DLk, and DLl, What is necessary is just to perform re-writing for the data read to the sense amplifier and data latch circuit DLj, DLk, and DLl each time after elimination for every control gate line. DRVd-DRVi is a control gate line and a selection gate line driver circuit, and BALd-BALi is a block address latch circuit.

[0072]Although drawing 20 is other examples of a circuit, this invention is effective, even when a verification circuit is shared with a write-in change confirmation circuit the whole bit in this way, the transistor count of a core part is reduced and reduction in a chip area is measured.
[0073]Although drawing 21 is an example of a circuit of further others, it may write in with an elimination change confirmation circuit in this way, and may share a verification circuit with a change confirmation circuit the whole bit. In this case, the power supply voltage VccVss of transistor Tr1 is set to Vcc the time of a write-in change check, and the whole bit at the time of verification, and is set to Vss at the time of an elimination change check. The verification circuit comprises a n channel MOS transistor the whole elimination change confirmation circuit and write-in change confirmation circuit and bit of drawing 21.
[0074]Next, the fourth example of this invention is described. As shown in threshold distribution of drawing 22, even if it performs verification writing the above whole bits, a threshold may be unable to be set as the predetermined range. For example, in NAND type EEPROM, "0" data is written in a selection cell and, in more than Vcc, the threshold presupposes then that it was set to 7V, for example. Next, though another cell of the NAND cell containing said selection cell is chosen and it tries to read data, since the cell more than Vcc exists in a non selection cell in a threshold, cell current does not flow. For this reason, regardless of the data of a selection cell, it always reads with "1" data and carries out, and it will be and will be judged with it being poor. That is, when it carries out even if it impresses Vcc to all the word lines of a NAND type cell, and cell current does not flow, in which cell in a selection NAND type cell, the threshold will have become exceeding the predetermined range more than Vcc. At this time, as shown in the voltage impressing figure of drawing 23, compulsive read voltage Vm0 of larger voltage than Vcc is impressed to a non selection word line or a selector gate, read voltage, for example, about 0.5V, is impressed to a selection word line, and a cell data is read. According to this data, a defective cell is relieved by carrying out re-writing for the same data to another block. At this time, said compulsive read voltage Vm0 is the voltage more than Vcc.
It is desirable that it is the same as the intermediate voltage impressed to the non selection control gate in selected blocks especially at the time of data writing.
The sequence of the operation described above is collectively shown in drawing 24.
[0075]Concrete operation of the fourth example described above is explained taking the case of a card system. The basic constitution of the card system of this example is the same as the system shown in drawing 7. That is, the external device is connected to the controller (CPU) 32 of the card system 30 via the interface 31. The memory system (in this case, 40') is connected with this CPU32 and the internal battery 33 to the timer 34. The method of operating within this memory system about the system which has the NAND type EEPROM cellular structure as memory structure. It explains to another block which leads the whole cell block connected with the same word line containing not only the cell that became poor but the cell which became poor to another word line taking the case of the case where re-writing is performed. Although a memory system here may comprise a single memory chip, it may serve as external out of a chip of a part of functions.
[0076]Drawing 25 is a block diagram showing the composition of memory system 40' of this example. The same number is given to the same block as drawing 8. First, the cell block which writes in data is chosen, the memory chip which should write in data is chosen by an internal address generation circuit, the control gate and bit line of the inside are chosen further, and the data which should be written in is further latched by the data input buffer. And 0V is impressed to all the control gates in a selection cell block by the writing operation timing control circuit 50, By the high voltage generation circuit 45, the high tension for elimination, for example, about 20V, is impressed to all the selector gates, the p type well, the n-type semiconductor board, and all the selector gates in a non selection cell block, and all the cells in a selection cell block are eliminated to them.
[0077]Next, in order to check an erasing state, erase verifying operation requires. Said erasing operation and erase verifying operation are repeated, and are performed until it impresses erasure

verifying voltage to all the control gates in a selection cell block, it reads data according to the usual read-out procedure and all the data turns into "1" data. Next, to the selection-control gate in a selection cell block by the writing operation timing control circuit 50 by the high voltage generation circuit 45. Impress the high tension for writing, for example, about 20V, and to the non selection control gate in a selection cell block by the intermediate voltage generating circuit 46. If it is "1" data, according to the data which impresses intermediate voltage, for example, about 10V, and has been latched to each bit line in said data input buffer circuit 53 by said intermediate voltage generating circuit 46. Intermediate voltage, for example, about 7V, is impressed, if it is "0" data, 0V is impressed, and data is written in.

[0078]Next, in order to check a writing state, write verification operation requires. Impress the first write verification voltage that judges the minimum of a threshold to the selection-control gate in a selection cell block, and in a non selection control gate. Said writing operation and write verification operation are repeated, and are performed until it impresses Vcc, it reads data according to the usual read-out procedure and all the data is in agreement with read data. Next, impress the second write verification voltage below Vcc which judges the maximum of a threshold to all the control gates in a selection cell block, and to a selector gate. Vcc is impressed, data is read for the voltage of each bit line by a sense amplifier circuit, the result is put into an I/O buffer, and it latches to data in a data latch circuit. Next, a data comparator circuit compares the value of the data latched in the data latch circuit. The threshold range check judging circuit 57 processes the comparison result, as shown below. If all the data is "1" data at this time, since data was written in the range of a normal threshold, it will end normally. On the other hand, if all the data does not turn into "1" data, it is judged that the threshold of at least one cell in selected blocks was written in exceeding the predetermined range, the flag which shows that a chip state is next in a relief state is set, and the re-writing of data is performed in the procedure shown below.

[0079]It assigns to the cell in the cell block which was protected by having made said selection cell block into the defective block, chose the following cell block, and chose the cell address in a former selection cell block by the memory cell array block control circuit 58 this time. And 0V is impressed to all the control gates in a new selection cell block by the writing operation timing control circuit 50, By the high voltage generation circuit 45, the high tension for elimination, for example, about 20V, is impressed to all the selector gates, the p type well, the n-type semiconductor board, and all the selector gates in a non selection cell block, and all the cells in a selection cell block are eliminated to them.

[0080]Next, in order to check an erasing state, erase verifying operation requires. Said erasing operation and erase verifying operation are repeated, and are performed until it impresses erasure verifying voltage to all the control gates in a selection cell block, it reads data according to the usual read-out procedure and all the data turns into "1" data. Next, after precharging all the bit lines connected to the pre-selection cell block to Vcc voltage by the read timing control circuit 52, Read voltage, for example, 0.5V, is impressed to the selection-control gate in a pre-selection NAND cell, and compulsive read voltage Vm0, for example, 10V, is impressed to it by the intermediate voltage generating circuit 46 at the non selection control gate in a selection NAND cell, and the selector gate in a selection NAND cell. And data is read for the voltage of each bit line by the sense amplifier circuit 43, the result is put into an I/O buffer, and data is latched to the data latch circuit 55 as compulsive read data.

[0081]Next, by the writing operation timing control circuit 50, to the selection-control gate in a new selection cell block by the high voltage generation circuit 45. Impress the high tension for writing, for example, about 20V, and to the non selection control gate in a new selection cell block by the intermediate voltage generating circuit 46. Impress intermediate voltage, for example, about 10V, and to each bit line. If it is "1" data, intermediate voltage, for example, about 7V, is impressed by said intermediate voltage generating circuit 46, according to the compulsive read data latched in said data latch circuit, if it is "0" data, 0V is impressed, and data is written in.

[0082]Next, in order to check a writing state, write verification operation requires. Said writing operation and write verification operation are repeated, and are performed until impress write verification voltage to the selection-control gate in a selection cell block, it impresses Vcc to a non selection control gate, it reads data according to the usual read-out procedure and all the data is in agreement with read data. Next, impress the second write verification voltage below Vcc which judges the maximum of a threshold to all the control gates in a selection cell block, and to a selector gate. Vcc is impressed, data is read for the voltage of each bit line by the sense amplifier circuit 43, the result is put into an I/O buffer, and it latches to data in the data latch circuit 55. Next, the value of the data latched in the data latch circuit is compared and carried out by the data comparator circuit 56. The threshold range check judging circuit 57 processes the comparison result, as shown below. Since data was written in the range of a normal threshold if all the data was "1" data at this time, re-writing operation is ended, the flag which shows that it is in a relief state is brought down, and all the threshold range check operations are ended. Threshold range check operation is performed until it carries out normal termination, if all the data does not turn into "1" data.

[0083]This invention is not limited to an above-mentioned example. In the above and an example, although nonvolatile semiconductor memories, such as EEPROM, were described, it may apply to the semiconductor memory device which accumulates an electric charge in a charge storage layer, and writes in "1" or "0" data, for example, a dynamic RAM etc. In said example, although data explained the case of the binary set to "1" and "0", in the case of the multiple value more than ternary, it may be applied. That is, as shown in drawing 26, the read voltage (Vr-N) corresponding to each data is received, Before and after that, to each data, the first threshold check voltage (Vv1-N), The read data (Data-N) in the read voltage (Vr-N) corresponding to [set up the second threshold check voltage (Vv2-N), and] each data like said example, The first confirmation data (Data-v1-N) based on the first threshold check voltage (Vv1-N) is compared with the second confirmation data (Data-v2-N) based on the second threshold check voltage (Vv2-N), and change of a threshold is detected. And when writing in the Nth data, the first threshold check voltage (Vv1-N) and the second threshold check voltage (Vv2-N) may be used for the voltage impressed at the time of a control gate at the time of the threshold verifying operation performed at the time of re-writing. At this time, a classification and a detection result as shown in Table 4 can be judged.

[0084]

[Table 4]

	しきい値状態	読み出しデータ	第1変動確認データ	第2変動確認データ	検知の結果
"N"データと"N+1"データが変動を確認する場合	Vv2-N+1≦Vth	"0"	"0"	"0"	"N+1"データが正常である
	Vr-N+1≦Vth<Vv2-N+1	"0"	"0"	"1"	"N+1"データが変動しているので"N+1"に再書き込み
	Vv1-N+1≦Vth<Vr-N+1	"0"	"1"	"1"	"N"データが変動しているので"N"に再書き込み
	Vth<Vv1-N+1	"1"	"1"	"1"	"N"データが正常である
"N"データと"N-1"データが変動を確認する場合	Vv2-N≦Vth	"0"	"0"	"0"	"N"データが正常である
	Vr -N≦Vth<Vv2-N	"0"	"0"	"1"	"N"データが変動しているので"N"に再書き込み
	Vv1-N≦Vth<Vr-N	"0"	"1"	"1"	"N-1"データが変動しているので"N-1"に再書き込み
	Vth<Vv1-N	"1"	"1"	"1"	"N-1"データが正常である

[0085]
[Effect of the Invention]By impressing the second voltage higher than the first voltage to a word line, reading a cell data in this invention, and comparing the cell data which impressed the first voltage to the word line and read it, When it judges that it is set as the range normal when these data is the same and these data differs on the other hand, data corruption has not been carried out, but it can be detected as carrying out threshold change enough. By impressing the third voltage lower than the first voltage to a word line, reading a cell data, and comparing the cell data which impressed the first voltage to the word line and read it, When it judges that it is set as the range normal when these data is the same and these data differs on the other hand, data corruption has not been carried out, but it can be detected as carrying out threshold change enough. When detected as changing the threshold of a cell enough, re-writing is performed for data so that it may return to the original threshold of each cell.
[0086]Thus, according to this invention, by threshold change, before data breaks, the threshold change is detected and it is corrected to the controlled original threshold.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application]This invention relates to a nonvolatile semiconductor memory (EEPROM) rewritable electric especially with respect to a semiconductor memory device.

[Translation done.]

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PRIOR ART

[Description of the Prior Art]NAND type EEPROM which can be integrated highly is known as one of the EEPROMs. This carries out the series connection of two or more memory cells in the form which shares those sauce and a drain by adjoining things, and connects them to a bit line as one unit. A memory cell usually has the FETMOS structure where the charge storage layer and the control gate were laminated. Accumulation formation of the memory cell array is carried out into the p type well formed in the p type substrate or the n type substrate. The drain side of a NAND cell is connected to a bit line via a selector gate, and the sauce side is too connected to a common source line via a selector gate. The control gate of a memory cell is continuously allocated in a line writing direction, and serves as a word line.
[0003]The operation of this NAND cell type EEPROM is as follows. Data writing impresses high-tension Vpp1 (about =20V) to the control gate of the selected memory cell, The intermediate voltage Vppm (about =10V) is impressed to the control gate and selector gate of a non selection memory cell, and 0V or the intermediate voltage Vm (about =8V) is given to a bit line according to data. When 0V is given to a bit line, the voltage is transmitted to the drain of a select memory cell, and electron injection produces it in an electric charge accumulation layer. This shifts the threshold of the selected memory cell for Masakata. This state is set to "0." When Vm is given to a bit line, electron injection does not happen effectually, therefore a threshold does not change but stops at negative. This state is set to "1" by an erasing state. Data writing is simultaneously performed to the memory cell which shares a control gate.
[0004]Data erasure is simultaneously performed to all the memory cells in a NAND cell. That is, all the control gates are set to 0V, and a p type well is set to Vpp2 (about =20V). At this time, a selector gate, a bit line, and a source line are also set to 20V. Thereby, the electrons of a charge storage layer are emitted to a p type well by all the memory cells, and a threshold is shifted to a negative direction.
[0005]Data read sets the control gate of the selected memory cell to 0V, and is performed by detecting whether current flows by a select memory cell by making the control gate and selector gate of the other memory cell into the power supply voltage Vcc (for example, 5V).
[0006]From restrictions of reading operation, the threshold after "0" writing must be controlled between 0V and Vcc. For this reason, write verification is performed, only the memory cell of "0" writing shortage is detected, and re-write data is set up so that re-writing may be performed only to the memory cell of "0" writing shortage (the whole bit is verified). The memory cell of "0" writing shortage is detected by setting the selected control gate to 0.5V (verification voltage), and reading it (verification read-out). That is, if the threshold of a memory cell has a margin to 0V and has not become more than 0.5V, current will flow by a select memory cell and it will be detected with "0" writing shortage. In the memory cell made into "1" writing state, since current naturally flows, the circuit called the verification circuit which compensates the current which flows through a memory cell is provided so that this memory cell may not be taken for "0" writing shortage. Write verification

is performed at high speed by this verification circuit.
[0007]Repeating writing operation and write verification, writing time is optimized to each memory cell by carrying out data writing, and the threshold after "0" writing is controlled between Vcc(s) from 0V.
[0008]By controlling a threshold between 0V and Vcc, NOR type EEPROM considers it as "1" data, and is taken as "0" data by controlling a threshold more than Vcc.
[0009]thus -- setting EEPROM at the time of data writing -- "0" and "1" -- it is alike, respectively, and it receives and a threshold is set up appropriately. However, it changes as time is formed as for the threshold of a memory cell. For example, since the electric charge of a charge storage layer decreases according to the leakage current of the surrounding insulator layer of a charge storage layer by being neglected after data is written in, it will change from the threshold set up appropriately to a neutral threshold. For example, in the case of NAND type EEPROM, if a neutral threshold shall be about 0.5 v, "1" data turns into "0" data, in the case of NOR type EEPROM, "0" data will turn into "1" data and data will be destroyed. Since it reads and Vcc voltage is sometimes impressed to a non selection cell, an electron is poured into a charge storage layer, "1" data turns into "0" data, and NAND type EEPROM has the problem that data is destroyed.
[0010]On the other hand, as mentioned above, even if it performs verification writing the whole bit, a threshold may be unable to be set as the predetermined range. For example, in NAND type EEPROM, "0" data is written in a selection cell and the threshold presupposes then that it became more than Vcc (for example, 7V). Next, in a non selection cell, though another cell of a NAND cell containing said selection cell is chosen and it tries to read data, since the cell more than Vcc exists, a threshold, Since cell current does not flow, in order to always read with "0" data regardless of the data of a selection cell, there is a problem of becoming poor.
[0011]Thus, in a nonvolatile semiconductor memory, there were a problem that data will be destroyed, and a problem of carrying out erroneous read if a threshold cannot be set as the predetermined range, by neglecting the written-in data.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention]By impressing the second voltage higher than the first voltage to a word line, reading a cell data in this invention, and comparing the cell data which impressed the first voltage to the word line and read it, When it judges that it is set as the range normal when these data is the same and these data differs on the other hand, data corruption has not been carried out, but it can be detected as carrying out threshold change enough. By impressing the third voltage lower than the first voltage to a word line, reading a cell data, and comparing the cell data which impressed the first voltage to the word line and read it, When it judges that it is set as the range normal when these data is the same and these data differs on the other hand, data corruption has not been carried out, but it can be detected as carrying out threshold change enough. When detected as changing the threshold of a cell enough, re-writing is performed for data so that it may return to the original threshold of each cell.
[0086]Thus, according to this invention, by threshold change, before data breaks, the threshold change is detected and it is corrected to the controlled original threshold.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]In the conventional nonvolatile semiconductor memory, there were a problem that data will be destroyed, and a problem of carrying out erroneous read if a threshold cannot be set as the predetermined range, by neglecting the written-in data as mentioned above.
[0013]The place which this invention was made in consideration of the above-mentioned situation, and is made into the purpose, This data by carrying out re-writing to the same block or another block by detecting change of the threshold of a memory cell and reading this data, The operation which makes it possible to set a threshold as the predetermined range and to avoid destruction of data, When it cannot be set as a predetermined threshold within the limits, this data by carrying out re-writing to the same block or another block by reading this data, It is in providing the semiconductor memory device possessing the operation which makes it possible to set a threshold as the predetermined range and to avoid erroneous read.

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MEANS

[Means for Solving the Problem]In order to solve an aforementioned problem, a semiconductor memory device of this invention, two or more arbitrary memory cells in a memory cell array by which a memory cell has been arranged on a semiconductor layer at matrix form, and said memory cell array -- or, In a semiconductor memory device provided with a threshold verification means to detect a threshold of two or more memory cells in said memory cell array connected with the same word line at least, When changing a threshold of at least one or more cells among said two or more memory cells is detected by said threshold verification means, it is characterized by providing operation which performs re-writing to said cell in which a threshold is changed at least.
[0015]A threshold state of two or more memory cells which stand in a row in the same word line in a memory cell array by impressing the first voltage to a selection word line specifically, The first operation that detects "1" data or "0" data, and the second operation that detects an upset condition of a threshold of two or more of said memory cells by impressing the second voltage higher than the first voltage to a selection word line, The third operation detected by impressing the third voltage lower than the first voltage to a selection word line, By comparing the first data of a memory cell which gave and read the first voltage to said word line with the second data of a memory cell which gave and read the second voltage higher than the first voltage to said word line, In a case where it is detected as the fourth operation that detects having changed in the direction with a small threshold of a memory cell, The fifth operation that fluctuates a threshold of the above-mentioned cell to a value higher than the second voltage, By comparing the first data of a memory cell which gave and read the first voltage to said word line with the third data of a memory cell which gave and read the third voltage lower than the first voltage to said word line, The sixth operation that detects having changed in the direction with a large threshold of a memory cell, When it detects, it is characterized by providing the seventh operation that fluctuates a threshold of the above-mentioned cell to a value lower than the third voltage.
[0016]While a threshold cannot be controlled in a predetermined range as erroneous read prevention, When a threshold is greatly set up across a prescribed range, With operation which impresses larger voltage than predetermined read voltage to a word line, and reads data, when a threshold is set up smaller than a prescribed range, Operation which impresses voltage smaller than predetermined read voltage to a word line, and reads data, and operation which carries out re-writing for this data to another block or the same block are provided.

[Translation done.]

OPERATION

[Function]By impressing the second voltage higher than the first voltage to a word line, reading a cell data in this invention, and comparing the cell data which impressed the first voltage to the word line and read it, When it judges that it is set as the range normal when these data is the same and these data differs on the other hand, data corruption has not been carried out, but it can be detected as carrying out threshold change enough. By impressing the third voltage lower than the first voltage to a word line, reading a cell data, and comparing the cell data which impressed the first voltage to the word line and read it, When it judges that it is set as the range normal when these data is the same and these data differs on the other hand, data corruption has not been carried out, but it can be detected as carrying out threshold change enough. When detected as changing the threshold of a cell enough, re-writing is performed for data so that it may return to the original threshold of each cell. Thus, according to this invention, by threshold change, before data breaks, the threshold change is detected and it is corrected to the controlled original threshold.
[0018]The next operation is performed while the threshold cannot be controlled in the predetermined range as erroneous read prevention. That is, when a threshold is greatly set up across a prescribed range, operation which impresses larger voltage than predetermined read voltage to a word line, and reads data is performed. When a threshold is set up smaller than a prescribed range, operation which impresses voltage smaller than predetermined read voltage to a word line, and reads data is performed. In NAND type EEPROM for example, by using this appearance, Though "0" data is written in a selection cell and the threshold has become more than Vcc (for example, 7V), Next, since sufficiently big voltage is impressed to the word line of this non selection cell even if the cell more than Vcc exists in a non selection cell in a threshold when another cell of a NAND cell containing said selection cell is chosen and data is read, it becomes possible to read the data of a selection cell correctly. this read data -- another block -- or the threshold of a memory cell can be set as the predetermined range by performing operation which carries out re-writing to the same block.

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EXAMPLE

[Example]Hereafter, an example is described, referring to drawings. Drawing 1 shows the superficial layout of the memory cell array of NAND cell type EEPROM concerning the first example of this invention, and drawing 2 and drawing 3 (a) and (b) show A-A' of drawing 1, and B-B' and the sectional view which met the C-C' line, respectively. The memory cell array of this example is formed on p type well 2b further formed in the n type well 2a formed on the p type semiconductor substrate 1 as shown in drawing 2. A memory cell may be directly formed on a p type semiconductor substrate.
[0020]In drawing 2, on p type well 2b, the charge storage layer 4 is formed via the 1st gate dielectric film 3, and the control gate 6 is further formed via the 2nd gate dielectric film 5. The n type diffused layers 7 are formed, it becomes the sauce and the drain area which the adjoining cell shares, and the memory cells M1-M4 connected in series are formed in the surface of said p type well 2b inserted into these lamination gate electrodes. The selection transistor S1 and S2 which have the selector gate 11 of a lamination type via gate-dielectric-film 3' on a p type well are formed in the right and left of these memory cells. On the control gate 6 and the selector gate 11, the bit line (BL) 10 is formed via the interlayer insulation film 9, the bit contacts 13 are led, and it is n+. It is connected to diffusion-zone 7'.
[0021]Although drawing 1 is the top view in which two rows of memory cell arrays like the above were shown, it is continuously connected to a transverse direction and the control gate 6 of the memory cell arranged in parallel serves as the control gate lines (word line) CG1-CG4. It is continuously connected to a transverse direction and the selector gate 11 is also set to selection gate line SG1 (drain side) and SG2 (sauce side). Between the selection transistor S1 connected to the bit line BL, and the selection transistor S2 connected to the common source line Vs, the series connection of the four memory cells M1-M4 is carried out, and they constitute one NAND cell. The selection transistor S1 and S2 have the selector gate SG. Like the above-mentioned, each memory cell has the floating gate 4 and the control gate 6 by which laminating formation was carried out, and memorizes information in the quantity of the electric charge stored in the floating gate 4. The quantity of this stored electric charge can be read as a threshold of a memory cell.
[0022]In this invention, detection of this threshold change is performed by the voltage impressing method shown in drawing 4 (a), (b), and (c). Here, the memory cell M2 which has control gate CG2 is chosen. Read to selection word line CG2 and the voltage 0.5V is impressed so that drawing 4 (a) may see, To non selection word line CG1, CG3, CG4 and the selection transistor S1, selector-gate SG1 of S2, and SG2, Vcc, For example, 5V is impressed, the common source line Vs, the p type substrate 1, and p type well 2b are grounded to 0V, and the bit line BL is precharged to Vcc and made into floating.
[0023]The threshold of the selection cell M2 reads, at this time, if it is more than voltage 0.5V, cell current does not flow, but the voltage of the bit line BL, The threshold of the selection cell M2 reads, on the other hand, it is maintained, if it is less than voltage 0.5V, cell current flows, and the

voltage of the bit line BL is set to 0V from a precharge level, has the voltage difference of this bit line, and detects it with a sense amplifier. At this time, use the time of bit line voltage being set to 0V as "1" data, and let one side be "0" data. Then, the read data of the detected cell is transmitted to latch circuitry from a sense amplifier, and latch circuitry is separated from a sense amplifier.
[0024]Next, while transmitting the latched data to I/O, the threshold fluctuation level shown below is checked. The first change check voltage 0.0V is impressed to selection word line CG2 so that drawing 4 (b) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs, the p type substrate 1, and p type well 2b are grounded to 0V, and the bit line BL is precharged to Vcc and made into floating.
[0025]At this time, if the threshold of the selection cell M2 is first more than change check voltage 0.0V, cell current does not flow, but the voltage of the bit line BL, It is maintained, on the other hand, if the threshold of the selection cell M2 is less than the first change check voltage 0.0V, cell current flows, and the voltage of the bit line BL is set to 0V from a precharge level. It has the voltage difference of this bit line, and the first change confirmation data is detected with a sense amplifier.
[0026]Next, the second change check voltage 1.0V is impressed to selection word line CG2 so that drawing 4 (c) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs, the p type substrate 1, and p type well 2b are grounded to 0V, and the bit line BL is precharged to Vcc and made into floating.
[0027]At this time, if the threshold of the selection cell M2 is second more than change check voltage 1.0V, cell current does not flow, The voltage of the bit line BL is maintained, on the other hand, if the threshold of the selection cell M2 is less than the second change check voltage 1.0V, cell current flows, and the voltage of the bit line BL is set to 0V from a precharge level. It has the voltage difference of this bit line, and the second change confirmation data is detected with a sense amplifier. At this time, as shown in Table 1, a classification and a detection result can be judged.
[0028]
[Table 1]

しきい値状態	読み出しデータ 図4(a)	第1の変動確認データ 図4(b)	第2の変動確認データ 図4(c)	検知の結果
1.0V<Vth	"0"	"0"	"0"	正常
0.5V<Vth≦1.0V	"0"	"0"	"1"	電子が放出された異常
0.0V<Vth≦0.5V	"1"	"0"	"1"	電子が注入された異常
0.0V>Vth	"1"	"1"	"1"	正常

First, read data is "0" when the threshold of a cell is more than 1.0V.
And the first change confirmation data is "0", and the second change confirmation data is set to "0."
Read data is "0" when the thresholds of a cell are more than 0.5V and less than 1.0V.
And the first change confirmation data is "0", and the second change confirmation data is set to "1."
Read data is "1" when the thresholds of a cell are more than 0.0V and more than 0.5V.
And the first change confirmation data is "0", and the second change confirmation data is set to "1."
Read data is "1" when the threshold of a cell is less than 0.0V.
And the first change confirmation data is "1", and the second change confirmation data is set to "1."

[0029]Below, the corrective action method for each of above-mentioned classifications is explained.

First, when the read-out data, first, and second change confirmation data is "0", originally "0" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made. When the read-out data, first, and second change confirmation data is "1", originally "1" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made.

[0030]On the other hand, read-out data and the first change confirmation data are "0", when the second change confirmation data is "1", originally "0" data is written in, but the threshold is changed from the positive threshold to the negative threshold.

It is not judged that the variation is large enough and data-hold is carried out normally, but re-writing is performed to a memory cell so that a threshold may be again shifted to a positive direction.

At this time, it is preferred to use the threshold more than said second change check voltage.

[0031]Read-out data and the second change confirmation data are "1", when the first change confirmation data is "0", originally "1" data is written in, but the threshold is changed from the negative threshold to the positive threshold.

It is not judged that the variation is large enough and data-hold is carried out normally, but re-writing is performed to a memory cell so that a threshold may be again shifted to a negative direction.

At this time, it is preferred to use the threshold below said first change check voltage. The sequence stated above is collectively shown in drawing 5.

[0032]Next, the re-writing operation performed according to the above-mentioned judgment is explained. Although only the cell which became poor may be re-written in, it does not matter even if it re-writes in the whole cell block containing the cell which became poor. When re-writing in for every cell block, the data in a cell block may be read once, and it may re-write in in the same cell block according to this data, and may re-write in in another cell block. The above-mentioned cell block may define it as two or more cells connected with the same word line, and may define it as two or more NAND cell blocks connected with the same word line. When abnormalities are detected by data fluctuation check operation following on the usual data reading operation, In order to go into re-writing operation, by setting a flag etc. shows that a chip state is in relief operation out of the chip by a chip being a waiting state like the usual method.

[0033]Whenever the data fluctuation check operation described above performs read operation of the selected cell data, may perform it to the cell block containing the selection cell and its selection cell, and, It is managed by the timer currently installed in a chip and out of the chip, and when predetermined time comes, it may be made to carry out to all the cells. Or when it is managed by the counter which counts the number of times of data read currently installed in a chip and out of the chip and only the predetermined number of times reads, it may be made to carry out to the cell or the cell block containing the cell. Although drawing 6 shows the block diagram of the card 20 containing CPU21 and the memory chip 22, The above-mentioned timer 23 or the counter 24 operates by an external power, when the external power 26 is supplied to the card, and when the external power is not supplied, it may be made to operate by the cell 25 installed on the card.

[0034]The card system based on the first example described above is shown in drawing 7. That is, the external device is connected to the controller (CPU) 32 of the card system 30 via the interface 31. The memory system 40 is connected with this CPU32 and the internal battery 33 to the timer 34. The method of operating within this memory system 40 about the case where it has the NAND type EEPROM cellular structure as memory structure. It explains to another block which leads the whole cell block connected with the same word line containing not only the cell that became poor but the cell which became poor to another word line taking the case of the case where re-writing is performed. Although a memory system here may comprise a single memory chip, it may serve as external out of a chip of a part of functions.

[0035]Drawing 8 is a block diagram showing the internal configuration of the memory system 40.

First, the cell block which performs a data fluctuation check is chosen, by the internal address generation circuit 51, the memory chip which should check data is chosen and the control gate and bit line of the inside are chosen further. And after precharging all the bit lines connected to the cell block to Vcc voltage by the read timing control circuit 52, Read voltage, for example, 0.5V, is impressed to the selection-control gate in a selection NAND cell, and Vcc voltage, for example, 3.3V, is impressed to it at the non selection control gate in a selection NAND cell, and the selector gate in a selection NAND cell. And data is read for the voltage of each bit line by the sense amplifier circuit 43, the result is put into I/O buffer 54, and data is latched to the data latch circuit 55 as read data.

[0036]Next, after precharging all the bit lines connected to the cell block to Vcc voltage by a change check operation timing control circuit, The first change check voltage, for example, 0.0V, is impressed to the selection-control gate in a selection NAND cell, and Vcc voltage, for example, 3.3V, is impressed to it at the non selection control gate in a selection NAND cell, and the selector gate in a selection NAND cell. And data is read for the voltage of each bit line by the sense amplifier circuit 43, the result is put into I/O buffer 54, and data is latched to the data latch circuit 55 as first change confirmation data.

Then, after precharging all the bit lines connected to the cell block to Vcc voltage, The second change check voltage, for example, 1.0V, is impressed to the selection-control gate in a selection NAND cell, and Vcc voltage, for example, 3.3V, is impressed to it at the non selection control gate in a selection NAND cell, and the selector gate in a selection NAND cell.

And data is read for the voltage of each bit line by the sense amplifier circuit 43, the result is put into I/O buffer 54, and data is latched to the data latch circuit 55 as second change confirmation data.

[0037]Next, the data comparator circuit 56 compares the value of the read data latched in the data latch circuit 55, the first change confirmation data, and the second change confirmation data. The change check operation judging circuit 57 processes the comparison result, as shown below. When all the read-out data, first, and second change confirmation data is "0", Originally "0" data is written in, and when all the read-out data, first, and second change confirmation data is "1", originally "1" data is written in, and it judges that data-hold is both carried out normally, and change check operation is ended. Read-out data and the first change confirmation data are "0", when the second change confirmation data is "1", originally "0" data is written in, but it is judged that a threshold is changed sharply. Read-out data and the second change confirmation data are "1", when the first change confirmation data is "0", originally "1" data is written in, but it is judged that a threshold is changed sharply.

[0038]As mentioned above, when the cell in which the threshold is changed is detected by the change check operation judging circuit 57, the flag which shows that a chip state is in a relief state is set, and the re-writing of data is performed in the procedure shown below. It assigns to the cell in the cell block which was protected by having made said selection cell block into the defective block, chose the following cell block, and chose the cell address in a former selection cell block by the memory cell array block control circuit this time. And 0V is impressed to all the control gates in a new selection cell block by the writing operation timing control circuit 50, By the high voltage generation circuit 45, the high tension for elimination, for example, about 20V, is impressed to all the selector gates, the p type well, the n-type semiconductor board (SUB), and all the selector gates in a non selection cell block, and all the cells in a selection cell block are eliminated to them.

[0039]Next, in order to check an erasing state, erase verifying operation requires. Said erasing operation and erase verifying operation are repeated, and are performed until it impresses erasure verifying voltage to all the control gates in a selection cell block, it reads data according to the usual read-out procedure and all the data turns into "1" data. At this time, it is most desirable to use the first change check voltage especially, using the voltage below the first change check voltage as erasure verifying voltage. Next, to the selection-control gate in a new selection cell block by the

writing operation timing control circuit 50 by the high voltage generation circuit 45. Impress the high tension for writing, for example, about 20V, and to the non selection control gate in a new selection cell block by the intermediate voltage generating circuit 46. Impress intermediate voltage, for example, about 10V, and to each bit line. If it is "1" data, intermediate voltage, for example, about 7V, is impressed by said intermediate voltage generating circuit 46, according to the data read data latched in said data latch circuit, if it is "0" data, 0V is impressed, and data is written in.

[0040]Next, in order to check a writing state, write verification operation requires. Impress write verification voltage to the selection-control gate in a selection cell block, and in a non selection control gate. Said writing operation and write verification operation are repeated, and are performed until it impresses Vcc, it reads data according to the usual read-out procedure and all the data is in agreement with read data. At this time, it is most desirable to use the second change check voltage especially, using the voltage more than the second change check voltage as write verification voltage. By the above, re-writing operation brings down the flag which shows that it ends and is in a relief state, and ends all the change check operations.

[0041]Although the above example is performed by [with read data] carrying out ternary comparison using the first and second change check voltage, When the changing direction of the threshold of a cell is decided, it is good in a line by carrying out binary comparison by using only either the first change check operation or the second change check operation. Below, it states concretely.

[0042]Next, the second example in connection with this invention is described. It performs the detection by a ****** case that this example changes the threshold of a cell in the direction of smallness by the voltage impressing method shown in drawing 9 (a) and (b). Here, the memory cell M2 which has control gate CG2 is chosen. Read to selection word line CG2 and the voltage 0.5V is impressed so that drawing 9 (a) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs and a p type substrate, or a p type well is grounded to 0V, and the bit line BL is precharged to Vcc and made into floating. At this time, the threshold of the ****** cell M2 reads, and, in the case of beyond voltage 0.5V, it does not flow through cell current, but the voltage of the bit line BL is maintained. On the other hand, the threshold of the selection cell M2 reads, in the case of not more than voltage 0.5V, cell current flows, the voltage of the bit line BL is set to 0V from a precharge level, and a sense amplifier detects the voltage difference of this bit line. At this time, use the time of bit line voltage being set to 0V as "1" data, and let another side be "0" data. Then, the read data of the detected cell is transmitted to latch circuitry from a sense amplifier, and latch circuitry is separated from a sense amplifier.

[0043]Next, while transmitting the latched data to I/O, the threshold fluctuation level shown below is checked. The first change check voltage 0.0V is impressed to selection word line CG2 so that drawing 9 (b) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs, the p type substrate 1, and p type well 2b are grounded to 0V, and the bit line BL is precharged to Vcc and made into floating. At this time, if the threshold of the selection cell M2 is first more than change check voltage 0.0V, cell current does not flow, but the voltage of the bit line BL, It is maintained, on the other hand, if the threshold of the selection cell M2 is less than the first change check voltage 0.0V, cell current flows, and the voltage of the bit line BL is set to 0V from a precharge level. It has the voltage difference of this bit line, and the first change confirmation data is detected with a sense amplifier. At this time, a classification and a detection result as shown in Table 2 can be judged.

[0044]

[Table 2]

しきい値状態	読み出しデータ 図9(a)	第1の変動確認データ 図9(b)	検知の結果
0.5V<Vth	"0"	"0"	正常
0.0V<Vth≦0.5V	"1"	"0"	電子が注入された異常
0.0V>Vth	"1"	"1"	正常

First, read data is "0" when the threshold of a cell is more than 0.5V.
And the first change confirmation data is "0."
Read data is "1" when the thresholds of a cell are more than 0.0V and more than 0.5V.
And the first change confirmation data is "0."
Read data is "1" when the threshold of a cell is less than 0.0V.
And the first change confirmation data is "1."

[0045]Below, the corrective action method for the above-mentioned classification is explained. First, when read-out data and the first change confirmation data are "0", originally "0" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made. When read-out data and the first change confirmation data are "1", originally "1" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made.
[0046]Read-out data is "1", the first change confirmation data is "0", and, in **, originally "1" data is written in, but the threshold is changed from the negative threshold to the positive threshold. It is not judged that the variation is large enough and data-hold is carried out normally, but the re-writing of data is performed like a last example.
Although the erasure verifying voltage used at the time of said erase verifying operation performed at this time may be below the first change check voltage, it is desirable to use the same voltage as the first change check voltage especially. As for the write verification voltage used at the time of said write verification operation, it is desirable to use the same voltage as read voltage. The sequence of the operation described above is collectively shown in drawing 10.
[0047]Next, the third example in connection with this invention is described. It performs the detection by a ****** case that this example changes the threshold of a cell in the adult direction by the voltage impressing method shown in drawing 9 (c) and (d). Here, the memory cell M2 which has control gate CG2 is chosen. Read to selection word line CG2 and the voltage 0.5V is impressed so that drawing 9 (c) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs, the p type substrate 1, and p type well 2b are grounded to 0V, and the bit line BL is precharged to Vcc and made into floating. At this time, the threshold of the selection cell M2 reads, and, in the case of beyond voltage 0.5V, it does not flow through cell current, but the voltage of the bit line BL is maintained. On the other hand, the threshold of the selection cell M2 reads, in the case of not more than voltage 0.5V, cell current flows, the voltage of the bit line BL is set to 0V from a precharge level, and a sense amplifier detects the voltage difference of this bit line. At this time, use the time of bit line voltage being set to 0V as "1" data, and let one side be "0" data. Then, the read data of the detected cell is transmitted to latch circuitry from a sense amplifier, and latch circuitry is separated from a sense amplifier.
[0048]Next, the second change check voltage 1.0V is impressed to selection word line CG2 so that drawing 9 (d) may see, Vcc, for example, 5V, is impressed to non selection word line CG1, CG3, CG4 and selector-gate SG1, and SG2, the common source line Vs and a p type substrate, or a p type well is grounded to 0V, and the bit line BL is precharged to Vcc and made into floating. At this time, when the threshold of the selection cell M2 is second more than change check voltage 1.0V, cell current does not flow, but the voltage of the bit line BL is maintained. On the other hand, when the

threshold of the selection cell M2 is less than the second change check voltage 1.0V, cell current flows, and the voltage of the bit line BL is set to 0V from a precharge level. It has the voltage difference of this bit line, and a sense amplifier detects the second change confirmation data. At this time, a classification and a detection result as shown in Table 3 can be judged.

[0049]

[Table 3]

しきい値状態	読み出しデータ 図9(c)	第2の変化確認データ 図9(d)	検知の結果
1.0V<Vth	"0"	"0"	正常
0.5V<Vth≦1.0V	"0"	"1"	電子が放出された異常
Vth≦0.5V	"1"	"1"	正常

First, read data is "0" when the threshold of a cell is more than 1.0V.
And the second change confirmation data is set to "0."
Read data is "0" when the thresholds of a cell are more than 0.5V and less than 1.0V.
And the second change confirmation data is set to "1."
Read data is "1" when the threshold of a cell is less than 0.5V.
And the second change confirmation data is set to "1."

[0050]Below, the corrective action method for the above-mentioned classification is shown. First, when read-out data and the second change confirmation data are "0", originally "0" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made. When read-out data and the second change confirmation data are "1", originally "1" data is written in, it judges that data-hold is carried out normally, and data correction to this cell is not made.

[0051]On the other hand, read-out data is "0", the second change confirmation data is "1", and, in **, originally "0" data is written in, but the threshold is changed from the positive threshold to the negative threshold.
It is not judged that the variation is large enough and data-hold is carried out normally, but the re-writing of data is performed like a last example.
As for the erasure verifying voltage used at the time of said erase verifying operation performed at this time, it is desirable to use the same voltage as read voltage. Although more than the second change check voltage may be sufficient as the write verification voltage used at the time of said write verification operation, it is desirable to use the same voltage as the second change check voltage especially. The sequence of the operation described above is collectively shown in drawing 11.

[0052]Only the size relation is important, and may make which voltage reference voltage, such as 0V and Vcc, and the read voltage described above, the first change detection voltage, and the second change detection voltage may apply NOR type EEPROM and a memory cell to AND type EEPROM connected in parallel.

[0053]Next, the circuit for realizing this invention concretely is explained. Drawing 12 is a precharge circuit, a write-in change confirmation circuit, an elimination change confirmation circuit, and an example of a circuit that includes a verification circuit, a sense amplifier and data latch circuit, and a package detecting circuit the whole bit. It writes in by p channel MOS transistorTr2 and Tr3, a change confirmation circuit is constituted, and the elimination change confirmation circuit comprises n channel MOS transistorTr4 and Tr5.

[0054]Drawing 13 is a circuit diagram for explaining detection of the abnormal data explained in drawing 4 and Table 1, and is taken as n=i, j, k, and l in a figure. i corresponds, when the read-out data [of the memory cell M2i], first, and second change confirmation data is "0" (i.e., when not

making data correction to M2i by the case where "0" data is originally written in and data-hold of it is carried out normally).
[0055]The read-out data of the memory cell M2j and the first change confirmation data are "0", when the second change confirmation data is "1", originally the data of "0" is written in, but j. It corresponds, when performing re-writing to the memory cell M2j by the case where the threshold is changed from the positive threshold to the negative threshold so that a threshold may be again shifted to a positive direction.
[0056]The read-out data of the memory cell M2k and the second change confirmation data are "1", when the first change confirmation data is "0", originally the data of "1" is written in, but k. It corresponds, when performing re-writing to the memory cell M2k by the case where the threshold is changed from the negative threshold to the positive threshold so that a threshold may be again shifted to a negative direction.
[0057]It corresponds, when the read-out memory cell [M2l.] data, first, and second change confirmation data of l is "1" (i.e., when not making data correction to M2l. by the case where the data of "1" is originally written in and data-hold of it is carried out normally).
[0058]Although the data of "1" is originally written in the memory cell M2k, drawing 14 and 15 divide a detection pickpocket operation timing figure two, and show the case where the threshold is changed from the negative threshold to the positive threshold. If the signal PRSTD for bit line reset changes from Vcc to Vss at first and bit line precharge signal PREB changes from Vcc to Vss, the bit line BLi, BLj, BLk, and BLl will be charged to bit line precharge level VR. At this time, the bit line transfer gate signal BLCD changes from Vss to Vcc, and the verification nodes VRYi, VRYj, and VRYk and VRYl are also charged to VR. Next, if control gating signal CG2 reads and control gating signal CG1 of others, CG3, CG4, selector-gate signal SG1, and SG2 are set to Vcc on the voltage VREAD (for example, 0.5V), the memory cell M2i, M2j, M2k, and M2l. will be read.
[0059]As for the memory cell M2i and M2j, originally "0" is written, since "1" is originally written, only the bit line BLkBLl is discharged and M2k and M2l. change from VR to Vss. When the control signal SEN of a sense amplifier and RLCH are set to Vcc from Vss after that and SENB and RLCHB are set to Vss from Vcc, Vcc is made the verification nodes VRYi and VRYj and Vss is latched to VRYk and VRYl (memory).
[0060]In order to read by the first check voltage VREF1 again after that, the bit line transfer gate signal BLCD is set to Vss from Vcc, and a bit line is separated from a verification node, and is charged to VR after bit line reset.
[0061]Next, if the first check voltage VREF1 (for example, 0V), control gating signal CG1 of others, CG3, CG4, selector-gate signal SG1, and SG2 turn into control gating signal CG2 to Vcc, the memory cell M2i, M2j, M2k, and M2l. will be read. Since the memory cell M2k is changed from the threshold negative in a threshold to the positive threshold at this time, the bit line BLk is not discharged. Other bit lines are the same as the case where read to the control gating signal CG2 [last], and the voltage VREAD is impressed and read.
[0062]Next, comparison with the last read-out data starts. The last read-out data is latched to the verification nodes VRYi, VRYj, and VRYk and VRYl. If the elimination acknowledge signal REFE of an elimination confirmation circuit is set to Vcc from Vss, the bit line BLiBLj is set to Vss from VR, and since the bit line BLl is Vss, only the bit line BLk will maintain precharge level VR. If the bit line transfer gate BLCD is set to Vcc from Vss after that and a bit line and a verification node connect too hastily, the bit line BLiBLj will become Vss+beta, BLk will become VR-alpha, and BLl will be set to Vss. When alpha and beta set capacity of a bit line and a verification node to CB and CVRY here, respectively, it is VR-alpha =-VRxCB/(CB+CVRY).
Vss+beta = (VccxCVRY)/(CB+CVRY)
It comes out, it is, and since CB is far large as compared with CVRY, VR-alpha becomes almost equal to VR, and Vss+beta is set to about 0 v.
[0063]Next, if the sense amplifier control signal SEN and RLCH are set to Vcc from Vss and SENB

and RLCHB are set to Vss from Vcc, only the verification node VRYk will be set to Vcc and other VRYi(s), VRYj, and VRYl will be set to Vss. If package detection reset-signal VSTIN is set to Vss from Vcc after that and the elimination detection signal AECON is set to Vcc from Vss, SENSE will be set to Vss from Vcc and will tell the abnormalities in read-out. If the abnormalities in read-out are told, the re-writing of a memory cell will start.

[0064]Although the data of "0" is originally written in the memory cell M2j, drawing 16 and 17 divide a detection pickpocket operation timing figure two, and show the case where the threshold is changed from the positive threshold to the negative threshold. If the signal PRSTD for bit line reset changes from Vcc to Vss at first and bit line precharge signal PREB changes from Vcc to Vss, the bit line BLi, BLj, BLk, and BLl will be charged to bit line precharge level VR. At this time, the bit line transfer gate signal BLCD changes from Vss to Vcc, and the verification nodes VRYi, VRYj, and VRYk and VRYl are also charged to VR. Next, if control gating signal CG2 reads and control gating signal CG1 of others, CG3, CG4, selector-gate signal SG1, and SG2 are set to Vcc on the voltage VREAD (for example, 0.5V), the memory cell M2i, M2j, M2k, and M2l. will be read.

[0065]As for the memory cell M2i and M2j, originally "0" is written, since "1" is originally written, only the bit line BLkBLl is discharged and M2k and M2l. change from VR to Vss. When the control signal SEN of a sense amplifier and RLCH are set to Vcc from Vss after that and SENB and RLCHB are set to Vss from Vcc, Vcc is made the verification nodes VRYi and VRYj and Vss is latched to VRYk and VRYl (memory).

[0066]In order to read by the second check voltage VREF2 again after that, the bit line transfer gate signal BLCD is set to Vss from Vcc, and a bit line is separated from a verification node, and is charged to VR after bit line reset.

[0067]Next, if the second check voltage VREF2 (for example, 1V), control gating signal CG1 of others, CG3, CG4, selector-gate signal SG1, and SG2 turn into control gating signal CG2 to Vcc, the memory cell M2i, M2j, M2k, and M2l. will be read. Since the memory cell M2j is changed from the threshold positive in a threshold to the negative threshold at this time, the bit line BLj is discharged. Other bit lines are the same as the case where read to the control gating signal CG2 [last], and the voltage VREAD is impressed and read.

[0068]Next, comparison with the last read-out data starts. The last read-out data is latched to the verification nodes VRYi, VRYj, and VRYk and VRYl. If the write-in acknowledge signal REFP of a write-in confirmation circuit is set to Vss from Vcc, the bit line BLkBLl is set to Vss from Vss, and since the bit line BLj is Vss, only the bit line BLi will maintain precharge level VR. If the bit line transfer gate BLCD is set to Vcc from Vss after that and a bit line and a verification node connect too hastily, the bit line BLkBLl will become Vcc-alpha, BLj will become Vss+beta, and BLi will be set to Vss. When alpha and beta set capacity of a bit line and a verification node to CB and CVRY here, respectively, it is Vcc-alpha =-(VccxCB)/(CB+CVRY).

Vss+beta = (VccxCVRY)/(CB+CVRY)

It comes out, it is, and since CB is far large as compared with CVRY, Vcc-alpha becomes almost equal to Vcc, and Vss+beta is set to about 0 v.

[0069]Next, if the sense amplifier control signal SEN and RLCH are set to Vcc from Vss and SENB and RLCHB are set to Vss from Vcc, only the verification node VRYj will be set to Vss and other VRYi(s), VRYk, and VRYl will be set to Vcc. If package detection reset-signal VSTIN is set to Vss from Vcc after that and the write-in detection signal APCON is set to Vcc from Vss, SENSE will be set to Vss from Vcc and will tell the abnormalities in read-out. If the abnormalities in read-out are told, the re-writing of a memory cell will start.

[0070]Drawing 18 and 19 divide the circuit block of a core part two, and show it, the blocks h and i are blocks of the spare for rewrites, and the other blocks d, e, and f and g are usually blocks. Now, the case where the abnormalities in read-out occur with the block d is considered. In this case, the stored data of the block d is copied to the SUPEA block h for re-writing, and the rewrite of the contents of the block h is carried out for the block d to the block d after block deletion. That is,

after carrying out block deletion of the spare block h first, it reads from control gate line CGd4 of the block d by read voltage VREAD. At this time, there are no abnormalities in read data, and even if there is change of a threshold, it is read correctly. These contents are latched to the sense-amplifier and data latch circuit DLj, DLk, and DLl. Control gate line CGh4 is chosen and the data latched to this sense-amplifier and data latch circuit DLj, DLk, and DLl is written in. This is repeated successively and the stored data about control gate line CGd4, CGd3, CGd2, and CGd1 is written in control gate line CGh4, CGh3, CGh2, and CGh1. Then, the contents of the stored data of the SUPEA block h are conversely re-written for the block d in the block d after block deletion.

[0071]When not block deletion but elimination of each page unit can be performed, Even if it does not use the SUPEA blocks h and i, it reads one contents about each control gate line of the block d at a time to the sense amplifier and data latch circuit DLj, DLk, and DLl, What is necessary is just to perform re-writing for the data read to the sense amplifier and data latch circuit DLj, DLk, and DLl each time after elimination for every control gate line. DRVd-DRVi is a control gate line and a selection gate line driver circuit, and BALd-BALi is a block address latch circuit.

[0072]Although drawing 20 is other examples of a circuit, this invention is effective, even when a verification circuit is shared with a write-in change confirmation circuit the whole bit in this way, the transistor count of a core part is reduced and reduction in a chip area is measured.

[0073]Although drawing 21 is an example of a circuit of further others, it may write in with an elimination change confirmation circuit in this way, and may share a verification circuit with a change confirmation circuit the whole bit. In this case, the power supply voltage VccVss of transistor Tr1 is set to Vcc the time of a write-in change check, and the whole bit at the time of verification, and is set to Vss at the time of an elimination change check. The verification circuit comprises a n channel MOS transistor the whole elimination change confirmation circuit and write-in change confirmation circuit and bit of drawing 21.

[0074]Next, the fourth example of this invention is described. As shown in threshold distribution of drawing 22, even if it performs verification writing the above whole bits, a threshold may be unable to be set as the predetermined range. For example, in NAND type EEPROM, "0" data is written in a selection cell and, in more than Vcc, the threshold presupposes then that it was set to 7V, for example. Next, though another cell of the NAND cell containing said selection cell is chosen and it tries to read data, since the cell more than Vcc exists in a non selection cell in a threshold, cell current does not flow. For this reason, regardless of the data of a selection cell, it always reads with "1" data and carries out, and it will be and will be judged with it being poor. That is, when it carries out even if it impresses Vcc to all the word lines of a NAND type cell, and cell current does not flow, in which cell in a selection NAND type cell, the threshold will have become exceeding the predetermined range more than Vcc. At this time, as shown in the voltage impressing figure of drawing 23, compulsive read voltage Vm0 of larger voltage than Vcc is impressed to a non selection word line or a selector gate, read voltage, for example, about 0.5V, is impressed to a selection word line, and a cell data is read. According to this data, a defective cell is relieved by carrying out re-writing for the same data to another block. At this time, said compulsive read voltage Vm0 is the voltage more than Vcc.

It is desirable that it is the same as the intermediate voltage impressed to the non selection control gate in selected blocks especially at the time of data writing.

The sequence of the operation described above is collectively shown in drawing 24.

[0075]Concrete operation of the fourth example described above is explained taking the case of a card system. The basic constitution of the card system of this example is the same as the system shown in drawing 7. That is, the external device is connected to the controller (CPU) 32 of the card system 30 via the interface 31. The memory system (in this case, 40') is connected with this CPU32 and the internal battery 33 to the timer 34. The method of operating within this memory system about the system which has the NAND type EEPROM cellular structure as memory structure. It explains to another block which leads the whole cell block connected with the same word line

containing not only the cell that became poor but the cell which became poor to another word line taking the case of the case where re-writing is performed. Although a memory system here may comprise a single memory chip, it may serve as external out of a chip of a part of functions.
[0076]Drawing 25 is a block diagram showing the composition of memory system 40' of this example. The same number is given to the same block as drawing 8. First, the cell block which writes in data is chosen, the memory chip which should write in data is chosen by an internal address generation circuit, the control gate and bit line of the inside are chosen further, and the data which should be written in is further latched by the data input buffer. And 0V is impressed to all the control gates in a selection cell block by the writing operation timing control circuit 50, By the high voltage generation circuit 45, the high tension for elimination, for example, about 20V, is impressed to all the selector gates, the p type well, the n-type semiconductor board, and all the selector gates in a non selection cell block, and all the cells in a selection cell block are eliminated to them.
[0077]Next, in order to check an erasing state, erase verifying operation requires. Said erasing operation and erase verifying operation are repeated, and are performed until it impresses erasure verifying voltage to all the control gates in a selection cell block, it reads data according to the usual read-out procedure and all the data turns into "1" data. Next, to the selection-control gate in a selection cell block by the writing operation timing control circuit 50 by the high voltage generation circuit 45. Impress the high tension for writing, for example, about 20V, and to the non selection control gate in a selection cell block by the intermediate voltage generating circuit 46. If it is "1" data, according to the data which impresses intermediate voltage, for example, about 10V, and has been latched to each bit line in said data input buffer circuit 53 by said intermediate voltage generating circuit 46. Intermediate voltage, for example, about 7V, is impressed, if it is "0" data, 0V is impressed, and data is written in.
[0078]Next, in order to check a writing state, write verification operation requires. Impress the first write verification voltage that judges the minimum of a threshold to the selection-control gate in a selection cell block, and in a non selection control gate. Said writing operation and write verification operation are repeated, and are performed until it impresses Vcc, it reads data according to the usual read-out procedure and all the data is in agreement with read data. Next, impress the second write verification voltage below Vcc which judges the maximum of a threshold to all the control gates in a selection cell block, and to a selector gate. Vcc is impressed, data is read for the voltage of each bit line by a sense amplifier circuit, the result is put into an I/O buffer, and it latches to data in a data latch circuit. Next, a data comparator circuit compares the value of the data latched in the data latch circuit. The threshold range check judging circuit 57 processes the comparison result, as shown below. If all the data is "1" data at this time, since data was written in the range of a normal threshold, it will end normally. On the other hand, if all the data does not turn into "1" data, it is judged that the threshold of at least one cell in selected blocks was written in exceeding the predetermined range, the flag which shows that a chip state is next in a relief state is set, and the re-writing of data is performed in the procedure shown below.
[0079]It assigns to the cell in the cell block which was protected by having made said selection cell block into the defective block, chose the following cell block, and chose the cell address in a former selection cell block by the memory cell array block control circuit 58 this time. And 0V is impressed to all the control gates in a new selection cell block by the writing operation timing control circuit 50, By the high voltage generation circuit 45, the high tension for elimination, for example, about 20V, is impressed to all the selector gates, the p type well, the n-type semiconductor board, and all the selector gates in a non selection cell block, and all the cells in a selection cell block are eliminated to them.
[0080]Next, in order to check an erasing state, erase verifying operation requires. Said erasing operation and erase verifying operation are repeated, and are performed until it impresses erasure verifying voltage to all the control gates in a selection cell block, it reads data according to the usual read-out procedure and all the data turns into "1" data. Next, after precharging all the bit lines

connected to the pre-selection cell block to Vcc voltage by the read timing control circuit 52, Read voltage, for example, 0.5V, is impressed to the selection-control gate in a pre-selection NAND cell, and compulsive read voltage Vm0, for example, 10V, is impressed to it by the intermediate voltage generating circuit 46 at the non selection control gate in a selection NAND cell, and the selector gate in a selection NAND cell. And data is read for the voltage of each bit line by the sense amplifier circuit 43, the result is put into an I/O buffer, and data is latched to the data latch circuit 55 as compulsive read data.

[0081]Next, by the writing operation timing control circuit 50, to the selection-control gate in a new selection cell block by the high voltage generation circuit 45. Impress the high tension for writing, for example, about 20V, and to the non selection control gate in a new selection cell block by the intermediate voltage generating circuit 46. Impress intermediate voltage, for example, about 10V, and to each bit line. If it is "1" data, intermediate voltage, for example, about 7V, is impressed by said intermediate voltage generating circuit 46, according to the compulsive read data latched in said data latch circuit, if it is "0" data, 0V is impressed, and data is written in.

[0082]Next, in order to check a writing state, write verification operation requires. Said writing operation and write verification operation are repeated, and are performed until impress write verification voltage to the selection-control gate in a selection cell block, it impresses Vcc to a non selection control gate, it reads data according to the usual read-out procedure and all the data is in agreement with read data. Next, impress the second write verification voltage below Vcc which judges the maximum of a threshold to all the control gates in a selection cell block, and to a selector gate. Vcc is impressed, data is read for the voltage of each bit line by the sense amplifier circuit 43, the result is put into an I/O buffer, and it latches to data in the data latch circuit 55. Next, the value of the data latched in the data latch circuit is compared and carried out by the data comparator circuit 56. The threshold range check judging circuit 57 processes the comparison result, as shown below. Since data was written in the range of a normal threshold if all the data was "1" data at this time, re-writing operation is ended, the flag which shows that it is in a relief state is brought down, and all the threshold range check operations are ended. Threshold range check operation is performed until it carries out normal termination, if all the data does not turn into "1" data.

[0083]This invention is not limited to an above-mentioned example. In the above and an example, although nonvolatile semiconductor memories, such as EEPROM, were described, it may apply to the semiconductor memory device which accumulates an electric charge in a charge storage layer, and writes in "1" or "0" data, for example, a dynamic RAM etc. In said example, although data explained the case of the binary set to "1" and "0", in the case of the multiple value more than ternary, it may be applied. That is, as shown in drawing 26, the read voltage (Vr-N) corresponding to each data is received, Before and after that, to each data, the first threshold check voltage (Vv1-N), The read data (Data-N) in the read voltage (Vr-N) corresponding to [set up the second threshold check voltage (Vv2-N), and] each data like said example, The first confirmation data (Data-v1-N) based on the first threshold check voltage (Vv1-N) is compared with the second confirmation data (Data-v2-N) based on the second threshold check voltage (Vv2-N), and change of a threshold is detected. And when writing in the Nth data, the first threshold check voltage (Vv1-N) and the second threshold check voltage (Vv2-N) may be used for the voltage impressed at the time of a control gate at the time of the threshold verifying operation performed at the time of re-writing. At this time, a classification and a detection result as shown in Table 4 can be judged.

[0084]

[Table 4]

	しきい値状態	読み出しデータ	第1変動確認データ	第2変動確認データ	検知の結果
"N"データと"N+1"データ変動を確認する場合	Vv2-N+1≦Vth	"0"	"0"	"0"	"N+1"データが正常である
	Vr-N+1≦Vth<Vv2-N+1	"0"	"0"	"1"	"N+1"データが変動しているので"N+1"に再書き込み
	Vv1-N+1≦Vth<Vr-N+1	"0"	"1"	"1"	"N"データが変動しているので"N"に再書き込み
	Vth<Vv1-N+1	"1"	"1"	"1"	"N"データが正常である
"N"データと"N-1"データ変動を確認する場合	Vv2-N≦Vth	"0"	"0"	"0"	"N"データが正常である
	Vr -N≦Vth<Vv2-N	"0"	"0"	"1"	"N"データが変動しているので"N"に再書き込み
	Vv1-N≦Vth<Vr-N	"0"	"1"	"1"	"N-1"データが変動しているので"N-1"に再書き込み
	Vth<Vv1-N	"1"	"1"	"1"	"N-1"データが正常である

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]The top view of the NAND type EEPROM memory cell array part concerning the first example of this invention.
[Drawing 2]The sectional view which met the A-A' line of drawing 1.
[Drawing 3]As for (a), (b) is the sectional view which met the B-B' line of drawing 1, and the sectional view which met the C-C' line of drawing 1.
[Drawing 4]The figure explaining the voltage impressing method at the time of the threshold change detection in the first example.
[Drawing 5]The figure explaining detection of the threshold change in the first example, and the sequence of relief.
[Drawing 6]The block diagram of the card in the first example.
[Drawing 7]The block diagram of the card system in the first example.
[Drawing 8]The block diagram of the memory system in drawing 7.
[Drawing 9](a) and (b) are the figures explaining the voltage impressing method at the time of threshold change detection [in / it is a figure explaining the voltage impressing method at the time of the threshold change detection in the second example, and / in (c) and (d) / the third example].
[Drawing 10]The figure explaining detection of the threshold change in the second example, and the sequence of relief.
[Drawing 11]The figure explaining detection of the threshold change in the third example, and the sequence of relief.
[Drawing 12]The concrete circuit diagram which realizes this invention.
[Drawing 13]The figure for explaining operation of drawing 12.
[Drawing 14]Some operation timing figures explaining 1 operation of drawing 13
[Drawing 15]The remaining portion explaining 1 operation of drawing 13 of an operation timing figure.

[Drawing 16]Some operation timing figures explaining operation of everything but drawing 13
[Drawing 17]The remaining portion explaining operation of everything but drawing 13 of an operation timing figure.
[Drawing 18]Some block diagrams of the core part of the semiconductor memory device of this invention
[Drawing 19]The remaining portion of the block diagram of the core part of the semiconductor memory device of this invention.
[Drawing 20]Other concrete circuit diagrams which realize this invention.
[Drawing 21]The concrete circuit diagram of further others which realizes this invention.
[Drawing 22]The figure explaining the abnormalities of threshold distribution.
[Drawing 23]The figure explaining the voltage impressing method at the time of the threshold change detection in the fourth example.

[Drawing 24]The figure explaining detection of the threshold change in the fourth example, and the sequence of relief.
[Drawing 25]The block diagram of the memory system in the fourth example.
[Drawing 26]The figure for explaining the method of a threshold change check of a multiple value.
[Description of Notations]
1 [-- The first insulator layer,] -- A p type semiconductor substrate, 2a -- A n type well, 2b -- A p type well, 3 4 [-- N type diffused layers,] -- A charge storage layer, 5 -- The second insulator layer, 6 -- A control gate, 7 8 [-- A selector gate, 13 / -- Bit line contact, 15 / -- A reversal prevention layer, S / -- A selection transistor, M / -- A memory cell, SG / -- A selector gate, CG / -- A control gate (word line), BL / -- A bit line, Vs / -- Source line voltage] -- An element isolation layer, 9 -- An interlayer insulation film, 10 -- A bit line, 11

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CORRECTION OR AMENDMENT

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[Amendment 1]
[Document to be Amended]Specification
[Item(s) to be Amended]Claim
[Method of Amendment]Change
[Proposed Amendment]
[Claim(s)]
[Claim 1]two or more arbitrary memory cells in a memory cell array by which a memory cell has been arranged on a semiconductor layer at matrix form, and said memory cell array -- or, In a semiconductor memory device provided with a threshold verification means to detect a threshold of

two or more memory cells in said memory cell array connected with the same word line at least,
First operation that impresses the first voltage to a selection word line for a threshold state of said memory cell, and detects "1" data or "0" data by said verification means,
Second operation that impresses the second voltage higher than the first voltage to a selection word line for an upset condition of a threshold of two or more of said memory cells, and detects "1" data and "0" data by said verification means,
Third operation that impresses the third voltage lower than said first voltage to a selection word line, and detects "1" data and "0" data by said verification means,
A semiconductor memory device comprising:
Data in which data of at least one or more cells impressed said first voltage to a selection word line, and read it among said two or more memory cells.
Fourth operation that performs re-writing to a cell which detects it as changing a threshold and is carrying out threshold change at least when data which impressed said second voltage to a selection word line, and read it is compared with data which impressed said third voltage to a selection word line, and read it and all are not in agreement.

[Claim 2]two or more arbitrary memory cells in a memory cell array by which a memory cell has been arranged on a semiconductor layer at matrix form, and said memory cell array -- or, In a semiconductor memory device provided with a threshold verification means to detect a threshold of two or more memory cells in said memory cell array connected with the same word line at least,
First operation that impresses the first voltage to a selection word line for a threshold state of said memory cell, and detects "1" data or "0" data by said verification means,
Second operation that impresses the second voltage that is different from the first voltage in an upset condition of a threshold of two or more of said memory cells to a selection word line, and detects "1" data and "0" data by said verification means,
A semiconductor memory device comprising:
Data in which data of at least one or more cells impressed said first voltage to a selection word line, and read it among said two or more memory cells.
Third operation that performs re-writing to a cell which compares data which impressed said second voltage to a selection word line, and read it, detects it as changing a threshold and is carrying out threshold change at least when not in agreement.

[Claim 3]two or more arbitrary memory cells in a memory cell array by which a memory cell has been arranged on a semiconductor layer at matrix form, and said memory cell array -- or, In a semiconductor memory device provided with a threshold verification means to detect a threshold of two or more memory cells in said memory cell array connected with the same word line at least,
First operation that impresses the first voltage to a selection word line for a threshold state of said memory cell, and detects "1" data or "0" data by said verification means,
Second operation that impresses the second voltage higher than the first voltage to a selection word line for an upset condition of a threshold of two or more of said memory cells, and detects "1" data and "0" data by said verification means,
Third operation that impresses the third voltage lower than said first voltage to a selection word line, and detects "1" data and "0" data by said verification means,
Fourth operation that detects having changed a threshold of a memory cell by comparing the first data of a memory cell which gave and read the first voltage to said word line with the second data of a memory cell which gave and read the second voltage higher than the first voltage to said word line,
Fifth operation that performs re-writing to a value higher than the second voltage to the above-mentioned cell at least when change is detected in said fourth operation,
Sixth operation that detects having changed a threshold of a memory cell by comparing the first

data of a memory cell which gave and read the first voltage to said word line with the third data of a memory cell which gave and read the third voltage lower than the first voltage to said word line,
A semiconductor memory device providing the seventh operation that performs re-writing to a value lower than the third voltage to the above-mentioned cell at least when change is detected in said sixth operation.
[Claim 4]Two or more data circuits which have a function to function as a sense amplifier and to memorize the inner first data of sensed information as data which controls a writing operation state of a memory cell,
A writing means for performing writing operation according to the contents of said first data circuit respectively corresponding to two or more memory cells in said memory cell array simultaneously,
A write verification means using said threshold detection means in order to check whether a state after writing operation of two or more of said memory cells is in a desired data storage state simultaneously,
The contents mass update means of a data circuit which carries out the mass update of the contents of the data circuit so that it may write in from the contents of the first data of a data circuit, and a state after writing operation of a memory cell and re-writing may be performed only to an insufficient memory cell,
Said contents mass update means of a data circuit so that bit line voltage may be sensed / memorized as re-write data, Voltage of a bit line with which a state after writing operation of a memory cell is outputted is corrected according to the contents of the data circuit, A data storage state of a data circuit is held until bit line voltage is corrected, A data circuit is operated as a sense amplifier, with corrected bit line voltage held, Perform a mass update of the contents of the data circuit and writing operation based on the contents and the contents mass update of a data circuit of a data circuit, The semiconductor memory device according to claim 4 providing further the eighth operation that performs data writing electrically by carrying out repeating until a memory cell will be in a predetermined writing state.

[Translation done.]